UCD3138A 用于隔离电源的高度集成数字控制器

1 器件概述

1.1 特性

- 可对多达 3 个独立反馈环路进行数字控制
  - 基于 PID 的专用硬件
  - 支持双极点/双零点配置
  - 非线性控制
- 带和不带预偏置电压的软启动/停止
- 快速输入电压前馈硬件
- 同步整流死区优化外设，可与 UCD7138 同步整流驱动器搭配使用
- 高达 16MHz 的误差模数转换器 (EADC)
  - 可配置低至 1mV/LSB 的分辨率
  - 自动分辨率选择
  - 高达 8 倍过度采样
  - 基于硬件的取平均值操作（高达 8 倍）
  - 带有 4 位抖动值的 10 位有效数模转换器 (DAC)
  - 自适应采样触发器定位
- 多达 8 个高分辨率数字脉宽调制 (DPWM) 输出
  - 250ps 脉宽分辨率
  - 4ns 频率和相位分辨率
  - 输出间的可调相移
  - 配对间的可调死区
  - 逐周期占空比匹配
  - 高达 2MHz 的切换频率
- 可配置的 PWM 边沿运动
  - 后缘调制
  - 前缘调制
  - 三角调制
- 可配置的反馈控制
  - 电压模式
  - 平均电流模式
  - 峰值电流模式控制
  - 恒定电流
  - 恒定电源
- 可配置调制方法
  - 频率调制
  - 相移调制
  - 脉宽调制
- 快速、自动且平滑的模式切换
  - 频率调制和 PWM
  - 相移调制和 PWM
  - 频率调制和相移调制
- 高效和轻负载管理
  - 突发模式
  - 理想的二极管仿真
  - 同步镇流器软打开/关闭
  - 低集成电路 (IC) 待机功率
- 初级侧电压感应
- 铜走线电流感应
- 磁通均衡和相电流均衡
- 电流共享总线支持
  - 平均模式或主从模式
- 特有丰富的故障保护选项
  - 7 个高速模拟比较器
  - 逐周期电流限制
  - 可编程故障输入
  - 外部故障中断功能
  - 10 个数字比较器
  - 可编程消隐时间
- 多个 UCD3138A 器件间的 DPWM 波形同步
- 14 通道、12 位、267ksps 通用 ADC
  - 可编程平均滤波器
  - 双采样保持
- 内部温度传感器
- 完全可编程的高性能 31.25MHz、32 位 ARM7TDMI-S™ 处理器
  - 32KB 程序闪存
  - 支持纠错码 (ECC) 的 2KB 数据闪存
  - 4KB 数据随机存取存储器 (RAM)
  - 可通过 I^2C 或通用异步收发器 (UART) 实现现场固件引导加载
- 通信外设
  - I^2C / 电源管理总线 (PMBus)
  - UCD3138RGC（64 引脚四方扁平无引线 (QFN)）上有 2 个 UART
  - UCD3138ARMH（40 引脚 QFN）上有 1 个 UART
- UART 自动波特率调整
- 具有可选输入引脚的定时器捕捉功能
- 多达 5 个附加的通用定时器
- 内置安全装置：BOD 和 POR
- 64 引脚和 40 引脚 QFN 封装
- 40 引脚 QFN 封装（通过 ICP9592A T/C 认证）
- 工作温度范围：-40°C 至 125°C
- 调试接口
  - Code Composer Studio™ （带 JTAG 接口）
  - Fusion Digital Power™ 设计人员GUI 支持

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.2 应用范围

- 电源和电信整流器
- 功率因数校正
- 独立的 DC-DC 模块

1.3 说明

UCD3138A 是一款德州仪器 (TI) 数字电源控制器，此控制器在一个单芯片解决方案内提供高集成度和优异的性能。 UCD3138A 灵活的特性使得此器件适用于广泛的电源转换应用。 此外，器件内的多种外设已经过专门优化，用于提升 AC/DC 和隔离式 DC/DC 应用性能并减少信息技术 (IT) 和网络基础设施空间内的解决方案组件数量。

UCD3138A 控制器是完全可编程的解决方案，可以使用户对相关应用实现完全控制，并且能够在同类解决方案中脱颖而出。 与此同时，德州仪器 (TI) 致力于通过提供一流的开发工具来简化用户的开发工作，其中包括应用固件、Code Composer Studio™ 软件开发环境和德州仪器 (TI) 的电源开发 GUI，这使得用户能够配置和监控关键系统参数。

UCD3138A 控制器的核心是数字控制环路外设，也称作数字电源外设 (DPP)。 每个 DPP 实现一个高速数字控制环路，此环路由专用误差模数转换器 (EADC)、基于 PID 的双极点/双零点数字补偿器以及脉宽分辨率为 250ps 的 DPWM 输出组成。 此器件还包含一个 12 位、267ksps 通用 ADC，此 ADC 具有多达 14 个通道、定时器、中断控制、PMBus 以及 UART 通信端口。 此器件基于一个32 位 ARM7TDMI-S 精简指令集计算机 (RISC) 微控制器，该微控制器可执行实时监控、配置外设以及管理通信。 ARM 微控制器从可编程闪存以及片上 RAM 和 ROM 执行其程序。

除了 DPP，该控制器还新增了专用电源管理外设，不仅可在整个工作范围内保持高效率，而且兼具高集成度（可提高功率密度）、高可靠性和最低总系统成本等优点，同时还能够灵活支持大量控制方案和拓扑结构。此类外设包括： 轻负载突发模式、同步整流、自动模式切换、输入电压前馈、铜走线电流感测、理想二极管仿真、恒定电流/恒定功率控制、同步整流软开启和关闭、峰值电流模式控制、磁通均衡、二次侧输入电压感测、高分辨率电流均流、带预偏置电压的硬件可配置软启动等。 已经针对电压模式和峰值电流模式受控相移全桥、单双相位功率因数校正 (PFC)、无桥 PFC、硬开关全桥和半桥、以及 LLC 半桥和全桥进行了拓扑支持优化。

UCD3138A 是 UCD3138 数字电源控制器的功能变型，相比 UCD3138 具有显著改进。 有关 UCD3138A 中的功能改进的完整说明，请参见《*UCD3138A 迁移指南*》。 主要改进如下：

提高了通用 ADC 在极低温度 (-40℃) 环境下的精度和性能。

UART 外设新增了基于硬件的自动波特率调整功能。

新增了同步整流死区优化硬件外设。 优势包括：

- 提高了效率
- 减小了同步整流电压应力
- 缩短了开发周期

添加了占空比读取功能，以便改善器件在峰值电流模式下的使用。

器件信息(1)

器件型号	封装	封装尺寸
UCD3138A	VQFN (64)	9.00mm x 9.00mm
	WQFN (40)(2)	6.00mm x 6.00mm

(1) 更多信息请参见节 9，*机械封装和可订购信息*。
(2) 40 引脚 6mm x 6mm x 0.75mm 超薄 QFN 封装，四角带有针对 IPC9592A 温度循环测试进行优化的固定点。

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1.4 功能方框图

图 1-1 显示器件的功能方框图。

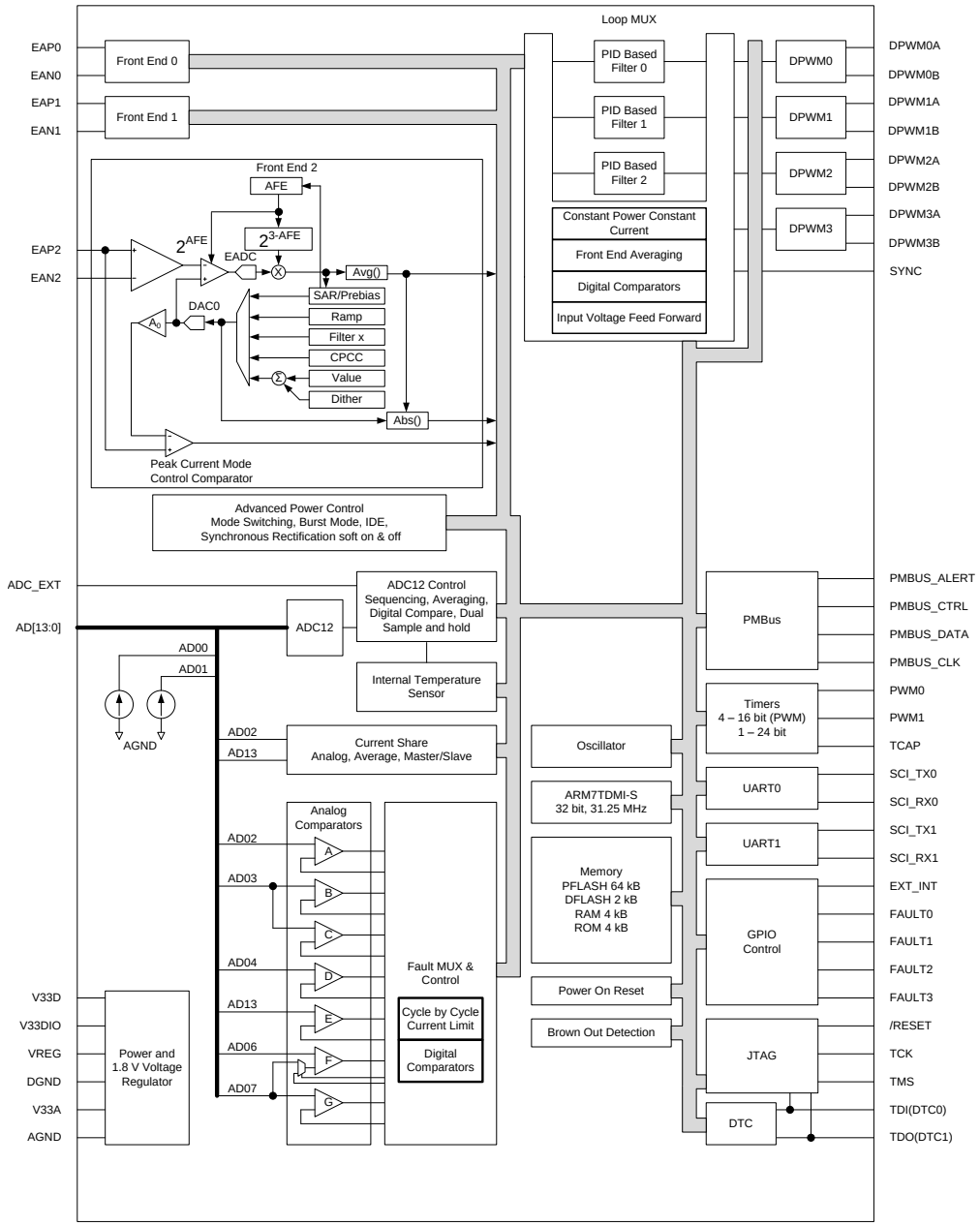

图 **1-1.** 功能框图

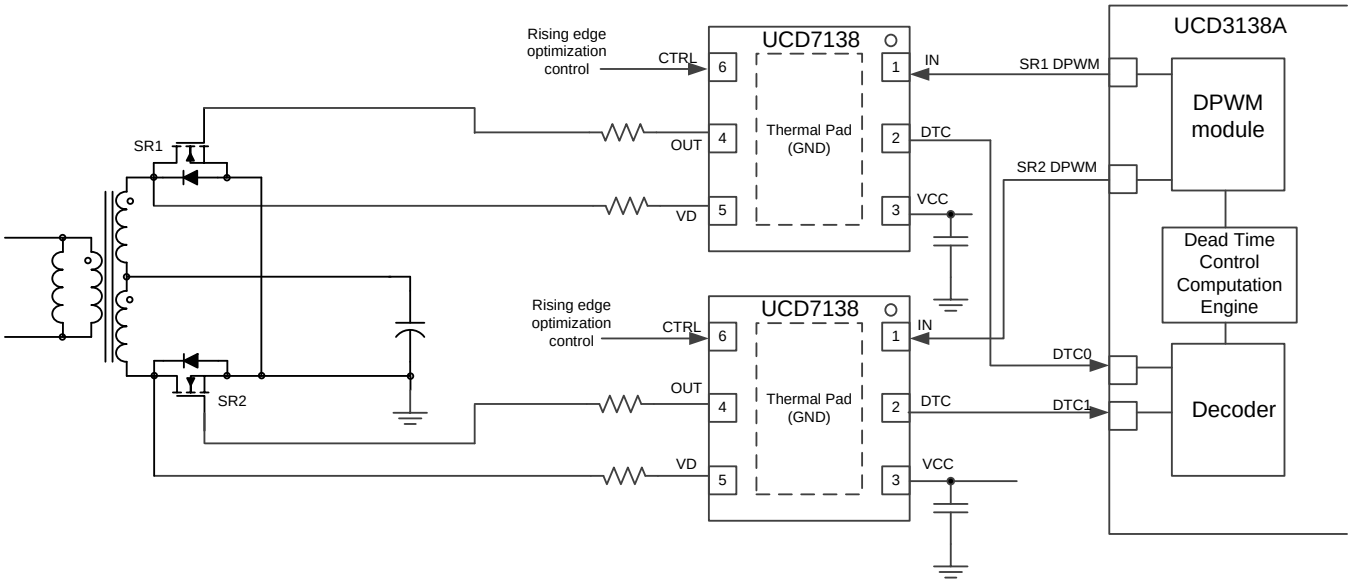

图 **1-2.** 同步整流外设与同步整流驱动器搭配使用

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2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2015) to Revision A **Page**

- 已将器件状态从“产品预览”更改为“量产” 1
- 已将*特性*中的“4kB 引导只读存储器 (ROM) 支持固件引导加载..”更改为 “可通过...” 1
- 已将*器件信息*表的注 2 从 “通过 IPC9592A 温度循环认证”更改为 “IPC9592A 温度循环测试。” 2
- Added Figure 5-3 17
- Changed Figure 5-9 23
- Changed Table 6-1 PRIORITY 19 From: CAPTURE_1_INT To: DTC_FLT_INT 29
- Changed Figure 6-1 to include DTC Adjustment 31
- Changed Figure 6-2 to include DTC Adjustment 32
- Changed Figure 6-3 to include DTC Adjustment 33

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3 Device Comparison

3.1 Product Selection Matrix

FEATURE	UCD3138A 64 PIN (RGC)	UCD3138A 40 PIN (RMH)
ARM7TDMI-S core processor	31.25 MHz	31.25 MHz
High resolution DPWM outputs (250-ps resolution)	8	8
Number of high speed independent feedback loops (number of regulated output voltages)	3	3
12-bit, 267ksps, general-purpose ADC channels	14	7
Digital comparators at ADC outputs	4	4
Flash memory (program)	32 kB	32 kB
Flash memory (data)	2 kB	2 kB
Flash security	√	√
RAM	4 kB	4 kB
DPWM switching frequency	up to 2 MHz	up to 2 MHz
Programmable fault inputs	4	1 + 2 (1)
High speed analog comparators with cycle-by-cycle current limiting	7 (2)	6 (2)
UART (SCI)	2	1 (1)
PMBus	√	√
Timers	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)
Timer PWM outputs	2	1
Timer capture inputs	1	1 (1)
Watchdog	√	√
On chip oscillator	√	√
Power-on reset and brown-out reset	√	√
Package offering	64 Pin VQFN (9 mm × 9 mm)	40 Pin WQFN (6 mm × 6 mm)
Sync IN and sync OUT functions	√	√
Total GPIO (includes all pins with multiplexed functions such as, DPWM, fault inputs, SCI, and so forth)	30	18
External interrupts	1	0

(1) This number represents an alternate pin out that is programmable via firmware. See the UCD3138A Digital Power Peripherals Programmer's Manual for details.
(2) To facilitate simple OVP and UVP connections both comparators B and C are connected to the AD03 pin.

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4 Terminal Configuration and Functions

4.1 UCD3138ARGC Package

64 QFN PACKAGE
TOP VIEW

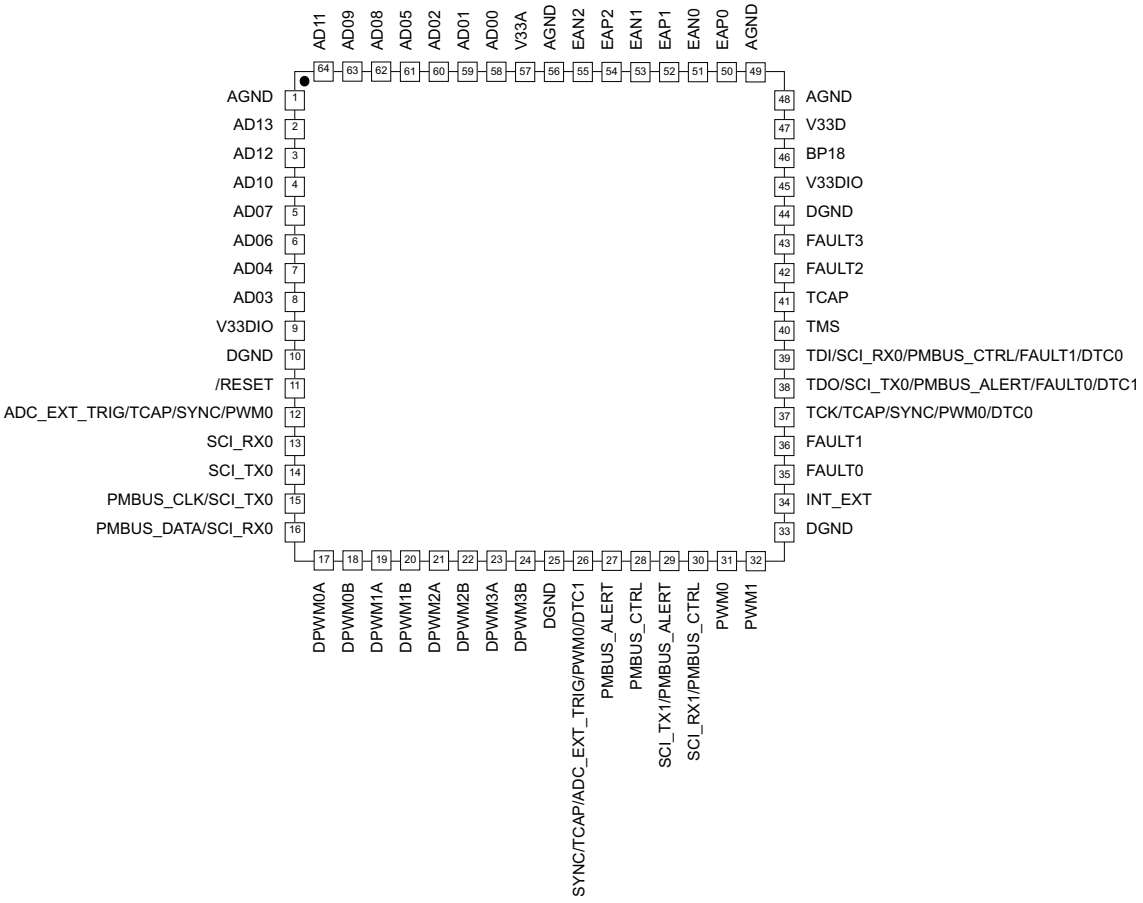

Table 4-1. UCD3138ARGC Terminal Functions

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT				CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	NO. 4	
1	AGND	Analog ground					
2	AD13	12-bit ADC, Ch 13, comparator E, I-share	DAC output				
3	AD12	12-bit ADC, Ch 12					
4	AD10	12-bit ADC, Ch 10					
5	AD07	12-bit ADC, Ch 7, Connected to comparator F and reference to comparator G	DAC output				
6	AD06	12-bit ADC, Ch 6, Connected to comparator F	DAC output				
7	AD04	12-bit ADC, Ch 4, Connected to comparator D	DAC output				
8	AD03	12-bit ADC, Ch 3, Connected to comparator B and C					
9	V33DIO	Digital I/O 3.3V core supply					
10	DGND	Digital ground					
11	$\overline{\text{RESET}}$	Device Reset Input, active low					
12	ADC_EXT_TRIG	ADC conversion external trigger input	TCAP	SYNC	PWM0		Yes
13	SCI_RX0	SCI RX 0					Yes
14	SCI_TX0	SCI TX 0					Yes
15	PMBUS_CLK	PMBUS Clock (Open Drain)	SCI TX 0				Yes
16	PMBUS_DATA	PMBus data (Open Drain)	SCI RX 0				Yes
17	DPWM0A	DPWM 0A output					Yes

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Table 4-1. UCD3138ARGC Terminal Functions (continued)

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT				CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	NO. 4	
18	DPWM0B	DPWM 0B output					Yes
19	DPWM1A	DPWM 1A output					Yes
20	DPWM1B	DPWM 1B output					Yes
21	DPWM2A	DPWM 2A output					Yes
22	DPWM2B	DPWM 2B output					Yes
23	DPWM3A	DPWM 3A output					Yes
24	DPWM3B	DPWM 3B output					Yes
25	DGND	Digital ground					
26	SYNC	DPWM Synchronize pin	TCAP	ADC_EXT_TRIG	PWM0	DTC1	Yes
27	PMBUS_ALERT	PMBus Alert (Open Drain)					Yes
28	PMBUS_CTRL	PMBus Control (Open Drain)					Yes
29	SCI_TX1	SCI TX 1	PMBUS_ALERT				Yes
30	SCI_RX1	SCI RX 1	PMBUS_CTRL				Yes
31	PWM0	General purpose PWM 0					Yes
32	PWM1	General purpose PWM 1					Yes
33	DGND	Digital ground					
34	INT_EXT	External Interrupt					Yes
35	FAULT0	External fault input 0					Yes
36	FAULT1	External fault input 1					Yes
37	TCK	JTAG TCK	TCAP	SYNC	PWM0	DTC0	Yes
38	TDO	JTAG TDO	SCI_TX0	PMBUS_ALERT	FAULT0	DTC1	Yes
39	TDI	JTAG TDI	SCI_RX0	PMBUS_CTRL	FAULT1	DTC0	Yes
40	TMS	JTAG TMS					Yes
41	TCAP	Timer capture input					Yes
42	FAULT2	External fault input 2					Yes
43	FAULT3	External fault input 3					Yes
44	DGND	Digital ground					
45	V33DIO	Digital I/O 3.3V core supply					
46	BP18	1.8V Bypass					
47	V33D	Digital 3.3V core supply					
48	AGND	Substrate analog ground					
49	AGND	Analog ground					
50	EAP0	Channel 0, differential analog voltage, positive input					
51	EAN0	Channel 0, differential analog voltage, negative input					
52	EAP1	Channel 1, differential analog voltage, positive input					
53	EAN1	Channel 1, differential analog voltage, negative input					
54	EAP2	Channel 2, differential analog voltage, positive input (Recommended for peak currrent mode control)					
55	EAN2	Channel #2, differential analog voltage, negative input					
56	AGND	Analog ground					
57	V33A	Analog 3.3-V supply					
58	AD00	12-bit ADC, Ch 0, Connected to current source					
59	AD01	12-bit ADC, Ch 1, Connected to current source					
60	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share					
61	AD05	12-bit ADC, Ch 5					
62	AD08	12-bit ADC, Ch 8					
63	AD09	12-bit ADC, Ch 9					
64	AD11	12-bit ADC, Ch 11					

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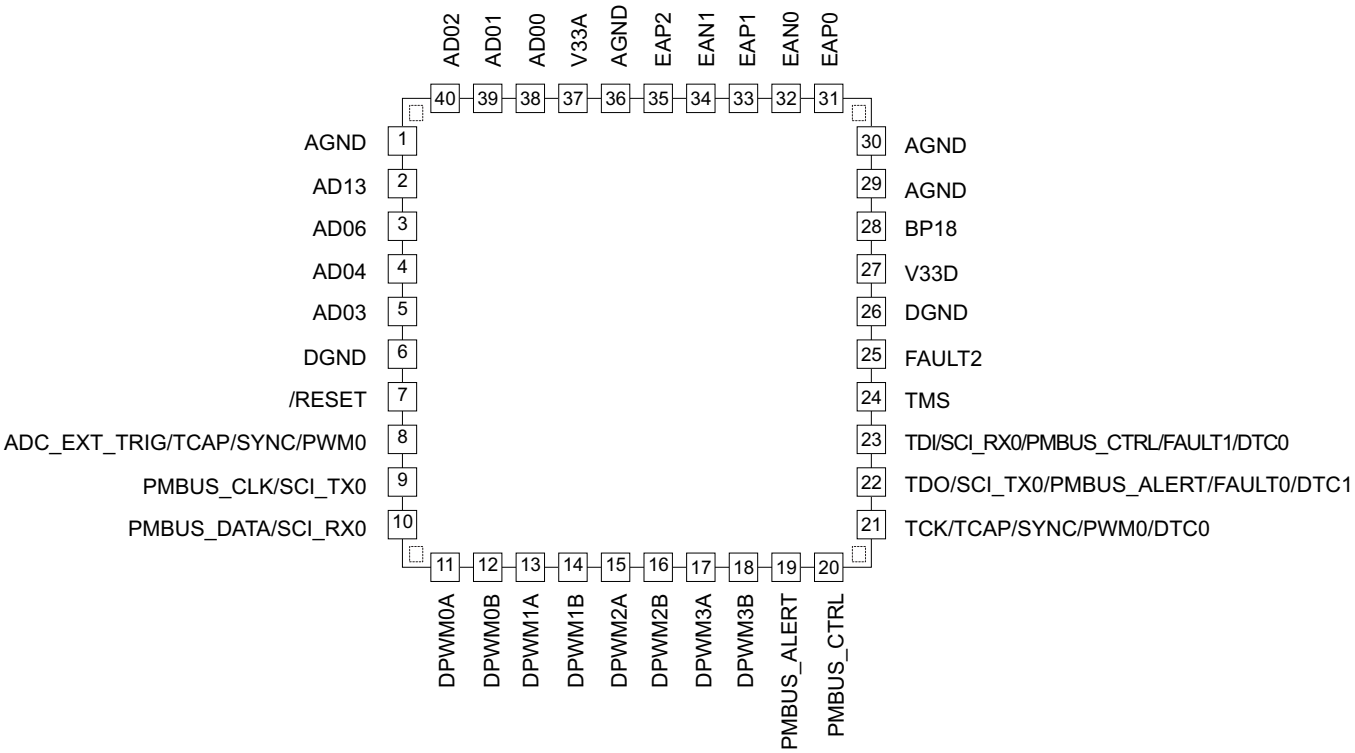
4.2 UCD3138ARMH Package

40 QFN PACKAGE
With Corner Anchors Pin Attributes
TOP VIEW



NOTE: The RMH package has thinner package height compared to the RHA package. There are also four corner pins on the RMH package. These features help to improve solder-joint reliability. The corner anchor pins and thermal pad should be soldered for robust mechanical performance and should be tied to the appropriate ground signal.

Table 4-2. UCD3138ARMH Terminal Functions

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT				CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	NO. 4	
1	AGND	Analog ground					
2	AD13	12-bit ADC, Ch 13, Connected to comparator E, I-share					
3	AD06	12-bit ADC, Ch 6, Connected to comparator F					
4	AD04	12-bit ADC, Ch 4, Connected to comparator D					
5	AD03	12-bit ADC, Ch 3, Connected to comparator B and C					
6	DGND	Digital ground					
7	$\overline{\text{RESET}}$	Device Reset Input, active low					
8	ADC_EXT_TRIG	ADC conversion external trigger input	TCAP	SYNC	PWM0		Yes
9	PMBUS_CLK	PMBUS Clock (Open Drain)	SCI_TX0				Yes
10	PMBUS_DATA	PMBus data (Open Drain)	SCI_RX0				Yes
11	DPWM0A	DPWM 0A output					Yes
12	DPWM0B	DPWM 0B output					Yes
13	DPWM1A	DPWM 1A output					Yes
14	DPWM1B	DPWM 1B output					Yes
15	DPWM2A	DPWM 2A output					Yes
16	DPWM2B	DPWM 2B output					Yes
17	DWPM3A	DPWM 3A output					Yes
18	DPWM3B	DPWM 3B output					Yes
19	PMBUS_ALERT	PMBus Alert (Open Drain)					Yes
20	PMBUS_CTRL	PMBus Control (Open Drain)					Yes
21	TCK	JTAG TCK	TCAP	SYNC	PWM0	DTC0	Yes

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Table 4-2. UCD3138ARMH Terminal Functions (continued)

PIN NO.	NAME	PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT				CONFIGURABLE AS A GPIO?
			NO. 1	NO. 2	NO. 3	NO. 4	
22	TDO	JTAG TDO	SCI_TX0	PMBUS_ALERT	FAULT0	DTC1	Yes
23	TDI	JTAG TDI	SCI_RX0	PMBUS_CTRL	FAULT1	DTC0	Yes
24	TMS	JTAG TMS					Yes
25	FAULT2	External fault input 2					Yes
26	DGND	Digital ground					
27	V33D	Digital 3.3V core supply					
28	BP18	1.8V Bypass					
29	AGND	Substrate analog ground					
30	AGND	Analog ground					
31	EAP0	Channel 0, differential analog voltage, positive input					
32	EAN0	Channel 0, differential analog voltage, negative input					
33	EAP1	Channel 1, differential analog voltage, positive input					
34	EAN1	Channel 1, differential analog voltage, negative input					
35	EAP2	Channel 2, differential analog voltage, positive input (Recommended for peak currrent mode control)					
36	AGND	Analog ground					
37	V33A	Analog 3.3-V supply					
38	AD00	12-bit ADC, Ch 0, Connected to current source					
39	AD01	12-bit ADC, Ch 1, Connected to current source					
40	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share					
Corner NA	Corner anchor pin	All four anchors should be soldered and tied to GND					

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	V33D to DGND	–0.3	3.8	V
	V33DIO to DGND	–0.3	3.8	V
	V33A to AGND	–0.3	3.8	V
	BP18 to DGND	–0.3	2.5	V
	Ground difference, |DGND – AGND|		0.3	V
	Applied to all pins, excluding AGND (2)	–0.3	3.8	V
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced to DGND

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Digital power, V33D	3	3.3	3.6	V
Digital I/O power, V33DIO	3	3.3	3.6	
Analog power, V33A	3	3.3	3.6	V
Junction temperature, T_J	–40		125	°C
1.8-V digital power, BP18	1.6	1.8	2	V

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5.4 Electrical Characteristics

V33A = V33D = V33DIO = 3 V to 3.6 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
	I33A	Measured on V33A. The device is powered up but all ADC12 and EADC sampling is disabled		6.3		mA
	I33DIO	All GPIO and communication pins are open		0.35		mA
	I33D	ROM program execution		60		mA
	I33D	Flash programming in ROM mode			70	mA
	I33	The device is in ROM mode with all DPWMs enabled and switching at 2 MHz. The DPWMs are all unloaded.			105	mA
ERROR ADC INPUTS EAP, EAN						
	EAP – AGND		–0.15		1.998	V
	EAP – EAN		–0.256		1.848	V
	Typical error range	AFE = 0	–256		248	mV
	EAP – EAN Error voltage digital resolution	AFE = 3	0.8	1	1.20	mV
		AFE = 2	1.7	2	2.30	mV
		AFE = 1	3.55	4	4.45	mV
		AFE = 0	6.90	8	9.10	mV
R_{EA}	Input impedance (See Figure 5-5)	AGND reference	0.5			MΩ
I_{OFFSET}	Input offset current (See Figure 5-5)		–5		5	µA
	EADC offset	Input voltage = 0 V at AFE = 0	–2		2	LSB
		Input voltage = 0 V at AFE = 1	–2.5		2.5	LSB
		Input voltage = 0 V at AFE = 2	–3		-3	LSB
		Input voltage = 0 V at AFE = 3	–4		4	LSB
	Sample Rate				16	MHz
	Analog Front End Amplifier Bandwidth			100		MHz
A_0	Gain	See Figure 5-6		1		V/V
	Minimum output voltage				30	mV
EADC DAC						
	DAC range		0		1.6	V
	VREF DAC reference resolution	10 bit, No dithering enabled		1.56		mV
	VREF DAC reference resolution	With 4 bit dithering enabled		97.6		µV
	INL		–3.0		3.0	LSB
	DNL	Does not include MSB transition	–2.1		1.6	LSB
	DNL at MSB transition			–1.4		LSB
	DAC reference voltage		1.58		1.61	V
τ	Settling Time	From 10% to 90%		250		ns
ADC12						
I_{BIAS}	Bias current for PMBus address pins		9.5		10.5	µA
	Measurement range for voltage monitoring		0		2.5	V
	Internal ADC reference voltage	–40°C to 125°C	2.475	2.500	2.525	V
	Change in Internal ADC reference from 25°C reference voltage(1)	–40°C to 25°C		–1.2		mV
		25°C to 125°C		–2.6		

(1) As designed and characterized. Not 100% tested in production.

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Electrical Characteristics *(continued)*

V33A = V33D = V33DIO = 3 V to 3.6 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	ADC12 INL integral nonlinearity, end point(2) (See Figure 5-3)	ADC_SAMPLINGSEL = 0 to 6 for all ADC12 data	–3.9	±2	4.5	LSB
	ADC12 INL integral nonlinearity, best fit(2) (See Figure 5-3)		–2.3	±1.5	2.6	LSB
	ADC12 DNL differential nonlinearity(2)			–0.8/+2.4		LSB
	ADC Zero Scale Error		–7		7	mV
	ADC Full Scale Error		–35		35	mV
	Input bias	2.5 V applied to pin			400	nA
	Input leakage resistance(1)	ADC_SAMPLINGSEL= 0 or 6		1		MΩ
	Input Capacitance(1)			10		pF
	ADC single sample conversion time(1)	ADC_SAMPLINGSEL= 0 or 6		3.9		µs
DIGITAL INPUTS/OUTPUTS(3)(4)						
V_{OL}	Low-level output voltage(5)	I_{OH} = 4 mA, V33DIO = 3 V			DGND + 0.25	V
V_{OH}	High-level output voltage (5)	I_{OH} = –4 mA, V33DIO = 3 V	V33DIO – 0.6			V
V_{IH}	High-level input voltage	V33DIO = 3 V	2.1			V
V_{IL}	Low-level input voltage	V33DIO = 3 V			1.1	V
I_{OH}	Output sinking current				4	mA
I_{OL}	Output sourcing current		–4			mA
SYSTEM PERFORMANCE						
TWD	Watchdog time out range	Total time is: TWD × (WDCTRL.PERIOD + 1)	14.6	17	20.5	ms
	Time to disable DPWM output based on active FAULT pin signal	High level on FAULT pin		70		ns
	Processor master clock (MCLK)			31.25		MHz
t_{Delay}	Digital compensator delay(6)	(1 clock = 32 ns)			6	clocks
$t_{(reset)}$	Pulse width needed at reset(1)		10			µs
	Retention period of flash content (data retention and program)	T_J = 25°C	100			years
	Program time to erase one page or block in data flash or program flash			20		ms
	Program time to write one word in data flash or program flash			20		µs
$f_{(PCLK)}$	Internal oscillator frequency		240	250	260	MHz
	Sync-in/sync-out pulse width	Sync pin		256		ns
	Flash Read			1		MCLKs
	Flash Write			20		µs
I_{SHARE}	Current share current source (See Figure 6-21)		238		259	µA
R_{SHARE}	Current share resistor (See Figure 6-21)		9.75		10.3	kΩ

(2) Minimum and maximum values are specified by design and characterization data.
(3) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset.
(4) On the 40-pin package V33DIO is connected to V33D internally.
(5) The maximum total current, IOHmax and I_{OLmax} for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –6 mA at V_{OL}; maximum source current per pin = 6 mA at V_{OH}.
(6) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay, which has no variation associated with it, must be accounted for when calculating the system dynamic response.

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Electrical Characteristics *(continued)*

V33A = V33D = V33DIO = 3 V to 3.6 V; 1 µF from BP18 to DGND, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER ON RESET AND BROWN OUT (V33D pin, See Figure 5-4)						
VGH		Voltage good high		2.7		V
VGL		Voltage good low		2.5		V
V_{res}		Voltage at which $I_{\overline{RESET}}$ signal is valid		0.8		V
T_{POR}		Time delay after power is good or $\overline{RESET}$ relinquished		1		ms
	Brownout	Internal signal warning of brownout conditions		2.9		V
TEMPERATURE SENSOR(7)						
V_{TEMP}		Voltage range of sensor	1.46		2.44	V
	Voltage resolution	V/°C		5.9		mV/ºC
	Temperature resolution	°C per bit		0.1034		ºC/LSB
	Accuracy(7)(8)	–40°C to 125°C	–10	±5	10	ºC
	Temperature range	–40°C to 125°C	–40		125	ºC
I_{TEMP}		Current draw of sensor when active		30		µA
T_{ON}		Turn on time / settling time of sensor		100		µs
V_{AMB}	Ambient temperature	Trimmed 25°C reading		1.85		V
ANALOG COMPARATOR						
DAC	Reference DAC Range		0		2.5	V
	Reference Voltage		2.478	2.5	2.513	V
	Bits			7		bits
	INL(7)		–0.42		0.21	LSB
	DNL(7)		0.06		0.12	LSB
	Offset		–5.5		19.5	mV
	Time to disable DPWM output based on 0 V to 2.5 V step input on the analog comparator.(1)				150	ns
	Reference DAC buffered output load(9)		0.5		1	mA
	Buffer offset (–0.5 mA)	0.3 V < DAC < 2.17 V	0		10	mV
	Buffer offset (1.0 mA)	0.3 V < DAC < 2.17 V	–10		0	mV

(7) Characterized by design and not production tested.
(8) Ambient temperature offset value should be used from the TEMPSENCTRL register to meet accuracy.
(9) Available from reference DACs for comparators D, E, F, and G.

5.5 Thermal Characteristics

THERMAL METRIC(1)		UCD3138A 64 PIN QFN (RGC)	UCD3138A 40 PIN QFN (RMH)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.1	31.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.5	16.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	6.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	
ψ_{JB}	Junction-to-board characterization parameter	4.6	6.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953

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5.6 PMBus/SMBus/I²C Timing

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus in Slave or Master mode are shown in Section 5.6, Figure 5-1, and Figure 5-2. The numbers in Section 5.6 arµe for 400 kHz operating frequency. However, the device supports all three speeds, standard (100 kHz), fast (400 kHz).

Typical values at T_A = 25°C and VCC = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle		100	400	kHz
f_{I2C}	I²C operating frequency	Slave mode, SCL 50% duty cycle		100	400	kHz
$t_{(BUF)}$	Bus free time between start and stop(1)			1.3		µs
$t_{(HD:STA)}$	Hold time after (repeated) start(1)			0.6		µs
$t_{(SU:STA)}$	Repeated start setup time(1)			0.6		µs
$t_{(SU:STO)}$	Stop setup time(1)			0.6		µs
$t_{(HD:DAT)}$	Data hold time	Receive mode		0		ns
$t_{(SU:DAT)}$	Data setup time			100		ns
$t_{(TIMEOUT)}$	Error signal/detect(2)				35	ms
$t_{(LOW)}$	Clock low period			1.3		µs
$t_{(HIGH)}$	Clock high period(3)			0.6		µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time(4)				25	ms
t_f	Clock/data fall time	Rise time t_r = (V_{ILmax} – 0.15) to (V_{IHmin} + 0.15)	20 + 0.1 Cb(5)		300	ns
t_r	Clock/data rise time	Fall time t_f = 0.9 VDD to (V_{ILmax} – 0.15)	20 + 0.1 Cb(5)		300	ns
C_b	Total capacitance of one bus line				400	pF

(1) Fast mode, 400 kHz
(2) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(3) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(4) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) C_b (pF)

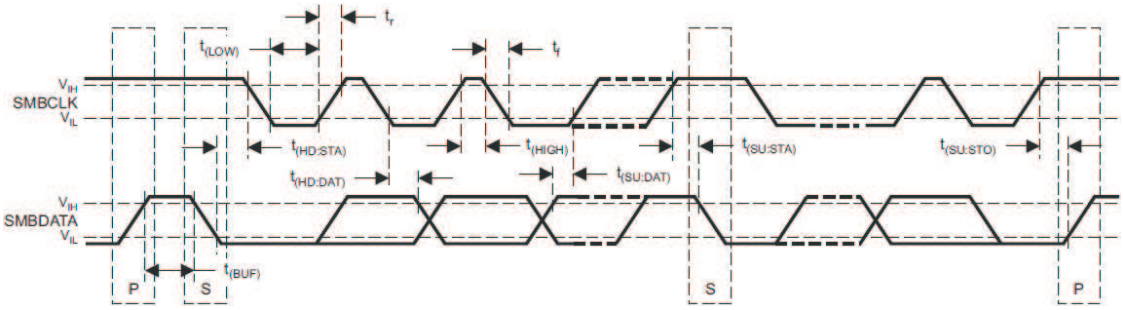

Figure 5-1. I²C/SMBus/PMBus Timing Diagram

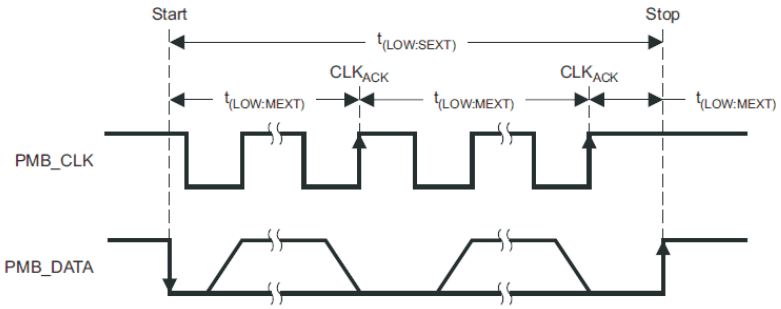

Figure 5-2. Bus Timing in Extended Mode

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5.7 Parametric Measurements Information

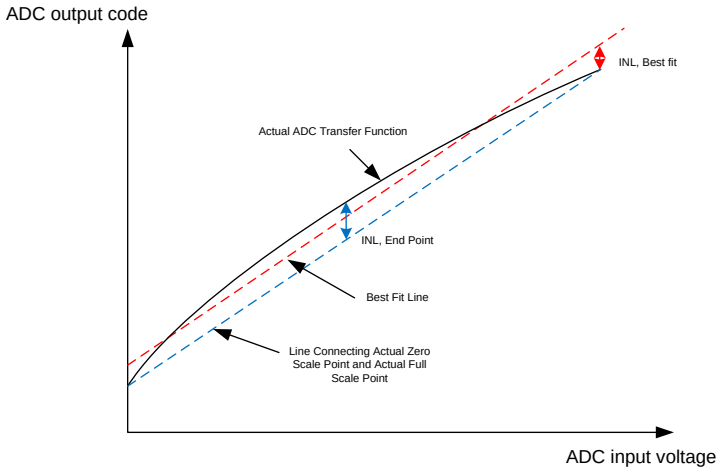

Figure 5-3. Best Fit INL and End Point INL

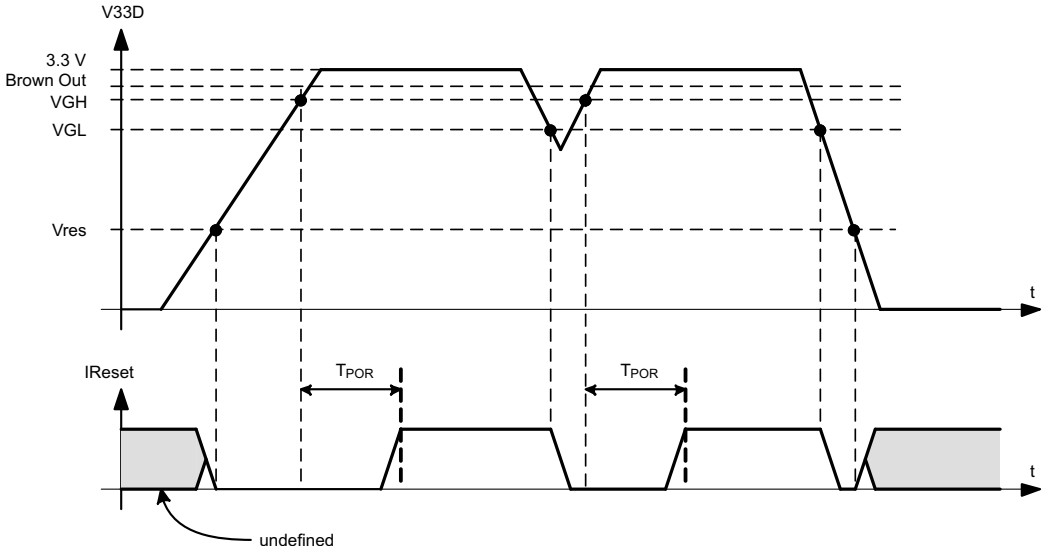

Figure 5-4. Power-On Reset (POR) and Brown-Out Reset (BOR)

VGH — This is the V33D threshold where the internal power is declared good. The UCD3138A comes out of reset when above this threshold.

VGL — This is the V33D threshold where the internal power is declared bad. The device goes into reset when below this threshold.

V_{res} — This is the V33D threshold where the internal reset signal is no longer valid. Below this threshold the device is in an indeterminate state.

I_{Reset} — This is the internal reset signal. When low, the device is held in reset. This is equivalent to holding the reset pin on the IC high.

T_{POR} — The time delay from when VGH is exceeded to when the device comes out of reset.

Brown out — This is the V33D voltage threshold at which the device sets the brown out status bit. In addition an interrupt can be triggered if enabled.

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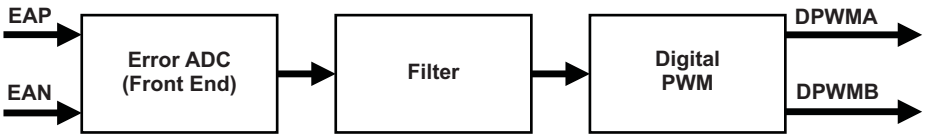
5.8 Peripherals

5.8.1 Digital Power Peripherals (DPPs)

At the core of the UCD3138A controller are three DDPs. Each DPP can be configured to drive from one to eight DPWM outputs. Each DPP consists of:

- Differential input error ADC (EADC) with sophisticated controls
- Hardware accelerated digital 2-pole/2-zero PID based compensator
- Digital PWM module with support for a variety of topologies

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, and so on. The simplest configuration is shown in the following figure:



5.8.1.1 Front End

Figure 5-5 shows the block diagram of the front end module. It consists of a differential amplifier, an adjustable gain error amplifier, a high speed flash analog to digital converter (EADC), digital averaging filters and a precision high resolution set point DAC reference. The programmable gain amplifier in concert with the EADC and the adjustable digital gain on the EADC output work together to provide 9 bits of range with 6 bits of resolution on the EADC output. The output of the Front End module is a 9-bit sign extended result with a gain of 1 LSB / mV. Depending on the value of AFE selected, the resolution of this output could be either 1, 2, 4 or 8 LSBs. In addition each EADC has the ability to automatically select the AFE value such that the minimum resolution is maintained that still allows the voltage to fit within the range of the measurement. The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC-9-bit-code and strobes the digital compensator for processing of the representative error. The set point DAC has 10 bits with an additional 4 bits of dithering resulting in an effective resolution of 14 bits. This DAC can be driven from a variety of sources to facilitate things like soft start, nested loops, and so on. Some additional features include the ability to change the polarity of the error measurement and an absolute value mode which automatically adds the DAC value to the error.

It is possible to operate the controller in a peak current mode control configuration; an EADC is recommended for implementing peak current mode control. In this mode, topologies like a phase shifted full bridge converter can be controlled to maintain transformer flux balance. The internal DAC can be ramped at a synchronously controlled slew rate to achieve a programmable slope compensation. This eliminates the sub-harmonic oscillation as well as improves input voltage feed-forward performance. A0 is a unity gain buffer used to isolate the peak current mode comparator. The offset of this buffer is specified in *Section 5.4*.

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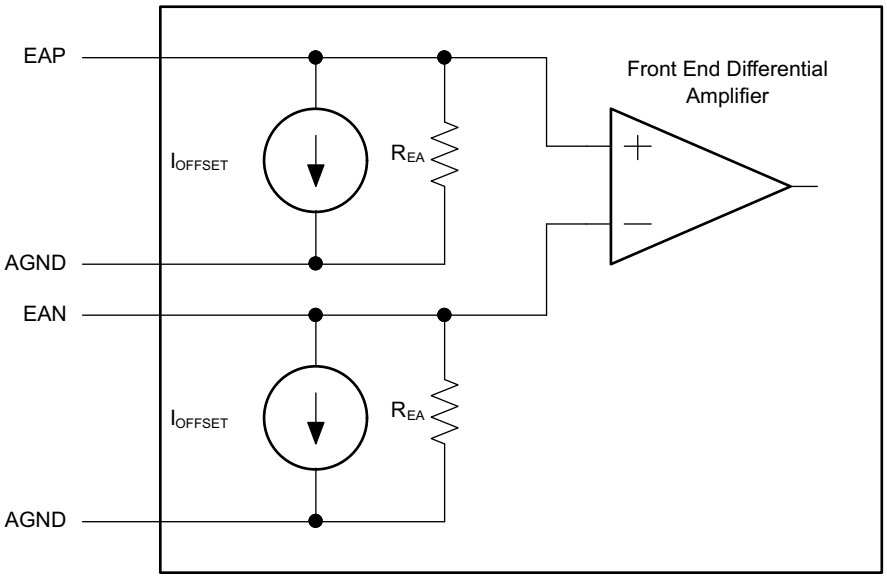

Figure 5-5. Input Stage of EADC Module

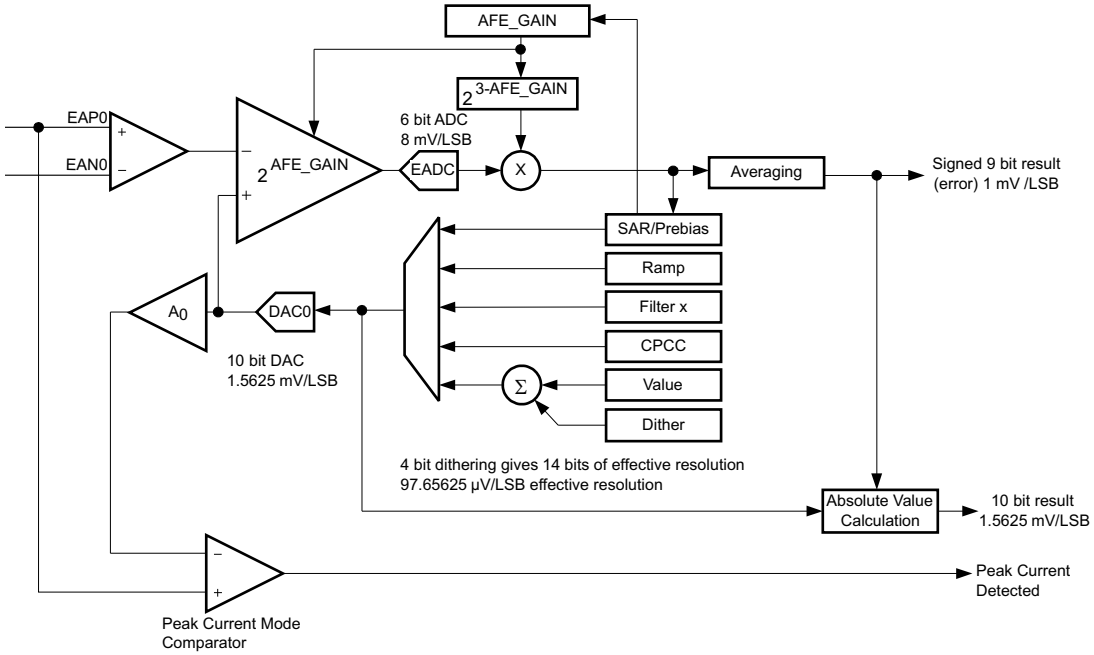

Figure 5-6. Front End Module
(Front End 2 Recommended for Peak Current Mode Control)

5.8.1.2 DPWM Module

The DPWM module represents one complete DPWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138A system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized DPWM—with user selectable phase shift between the DPWM channels to control power supply outputs with multiphase or interleaved DPWM configurations.

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The output of the filter feeds the high resolution DPWM module. The DPWM module produces the pulse width modulated outputs for the power stage switches. The compensator calculates the duty ratio as a 24-bit number in Q23 fixed point format (23 bit integer with 1 sign bit). This represents a value within the range 0.0 to 1.0. This duty ratio value is used to generate the corresponding DPWM output ON time. The resolution of the DPWM ON time is 250 psec.

Each DPWM module can be synchronized to another module or to an external sync signal. An input SYNC signal causes a DPWM ramp timer to reset. The SYNC signal outputs—from each of the four DPWM modules—occur when the ramp timer crosses a programmed threshold. In this way the phase of the DPWM outputs for multiple power stages can be tightly controlled.

The DPWM logic is probably the most complex of the Digital Peripherals. It receives the output of the compensator and converts it into the correct DPWM output for several power supply topologies. It provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. It can provide synchronization information to other DPWMs or to external recipients. In addition, it interfaces to several fault handling circuits. Some of the control for these fault handling circuits is in the DPWM registers. Fault handling is covered in the Fault Mux section.

Each DPWM module supports the following features:

- Dedicated 14 bit time-base with period and frequency control
- Shadow period register for end of period updates.
- Quad-event control registers (A and B, rising and falling) (Events 1 to 4)
  - Used for on/off DPWM duty ratio updates.
- Phase control relative to other DPWM modules
- Sample trigger placement for output voltage sensing at any point during the DPWM cycle.
- Support for two independent edge placement DPWM outputs (same frequency or period setting)
- Dead-time between DPWM A and B outputs
- High Resolution capabilities – 250 ps
- Pulse cycle adjustment of up to ±8.192 µs (32768 × 250 ps)
- Active high/ active low output polarity selection
- Provides events to trigger both CPU interrupts and start of ADC12 conversions.

5.8.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*–This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. The clock controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase Trigger Count* – count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period* – low resolution switching period count. (count of PCLK cycles)
4. *Event 1* – count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust* – Constant offset for Event 2 and Event 4 adjustments.

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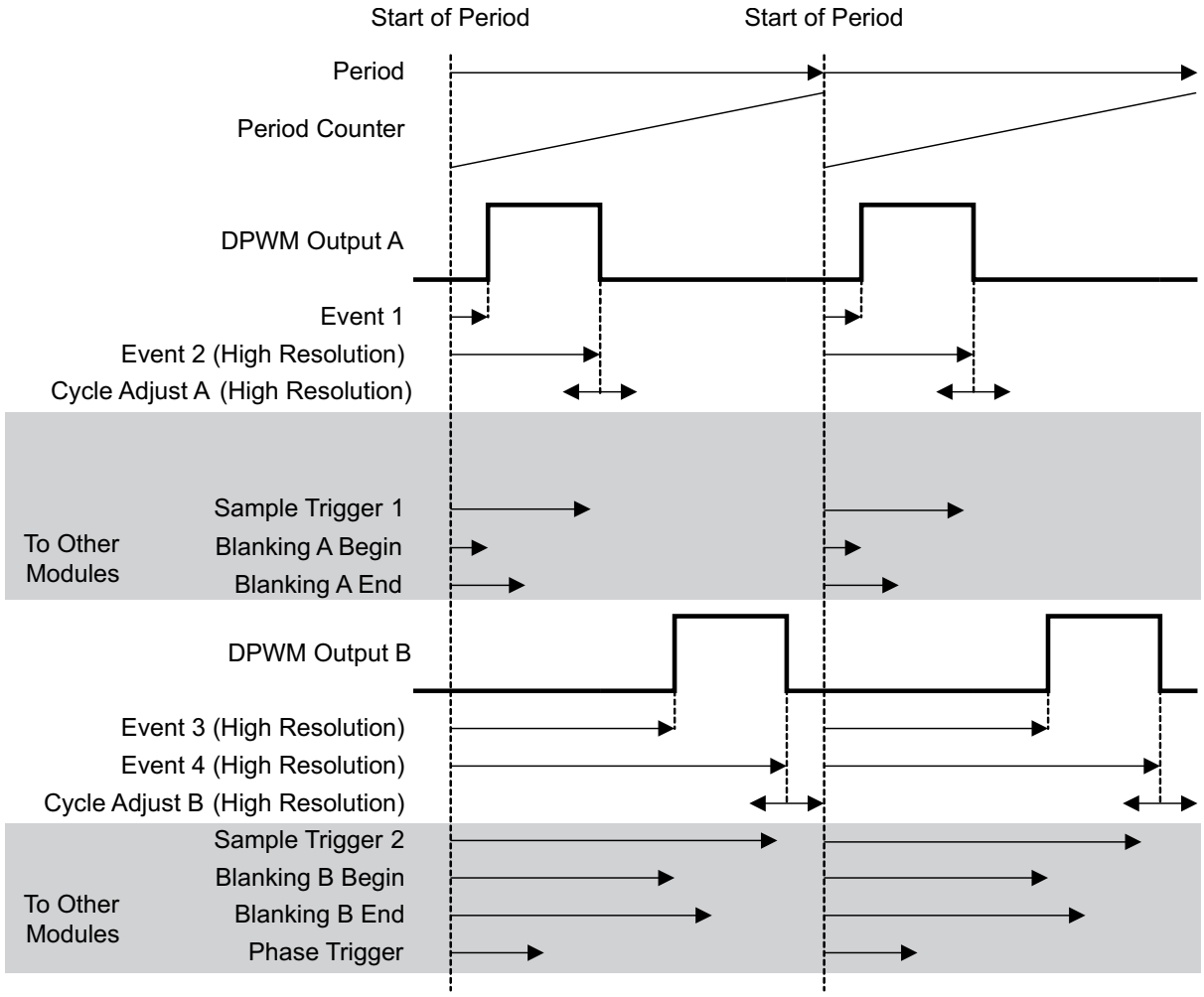
Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3, and 4.

Figure 5-7 is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

The Sample Trigger signals are used to trigger the front end to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off.



Events which change with DPWM mode:

- DPWM A Rising Edge = Event 1
- DPWM A Falling Edge = Event 2 + Cycle Adjust A
- DPWM B Rising Edge = Event 3
- DPWM B Falling Edge = Event 4 + Cycle Adjust B
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 5-7. Multi Mode Open Loop

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5.8.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138A DPWM can generate waveforms with resolutions as small as 250 ps. This is 16× the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz. The high resolution section of DPWM can be enabled or disabled, and the resolution can be defined in several steps between 4 ns to 250 ps. This is done by setting the values of PWM_HR_MULTI_OUT_EN and HIRES_SCALE inside the DPWM Control register 1. See the Power Peripherals programmer's manual for details.

5.8.1.5 Oversampling

The DPWM module has the capability to trigger an oversampling event by initiating the EADC to sample the error voltage. The default 00 configuration has the DPWM trigger the EADC once based on the sample trigger register value. The over sampling register has the ability to trigger the sampling 2, 4 or 8 times per PWM period. Thus the time the over sample happens is at the divide by 2, 4, or 8 time set in the sampling register. The 01 setting triggers 2X oversampling, the 10 setting triggers 4X over sampling, and the 11 triggers oversampling at 8X.

5.8.1.6 DPWM Interrupt Generation

The DPWM has the capability to generate a CPU interrupt based on the PWM frequency programmed in the period register. The interrupt can be scaled by a divider ratio of up to 255 for developing a slower interrupt service execution loop. This interrupt can be fed to the ADC circuitry for providing an ADC12 trigger for sequence synchronization. Table 5-1 outlines the divide ratios that can be programmed.

5.8.1.7 DPWM Interrupt Scaling/Range

Table 5-1. DPWM Interrupt Divide Ratio

Interrupt Divide Setting	Interrupt Divide Count	Interrupt Divide Count (hex)	Switching Period Frames (Assume 1-MHz Loop)	Number of 32-MHz Processor Cycles
1	0	00	1	32
2	1	01	2	64
3	3	03	4	128
4	7	07	8	256
5	15	0F	16	512
6	31	1F	32	1024
7	47	2F	48	1536
8	63	3F	64	2048
9	79	4F	80	2560
10	95	5F	96	3072
11	127	7F	128	4096
12	159	9F	160	5120
13	191	BF	192	6144
14	223	DF	224	7168
15	255	FF	256	8192

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5.8.1.8 Synchronous Rectifier Dead Time Optimization Peripheral

The UCD3138A has an advanced dead time control interface where it can accept UCD7138 output signals and optimize SR gate driver signals accordingly. The UCD7138 low-side MOSFET driver is a high-performance driver for secondary-side synchronous rectification (SR) with body diode conduction sensing. The device is suitable for high power high efficiency isolated converter applications where dead-time optimization is desired. The UCD7138 gate driver is a companion device to UCD3138A highly integrated digital controller for isolated power.

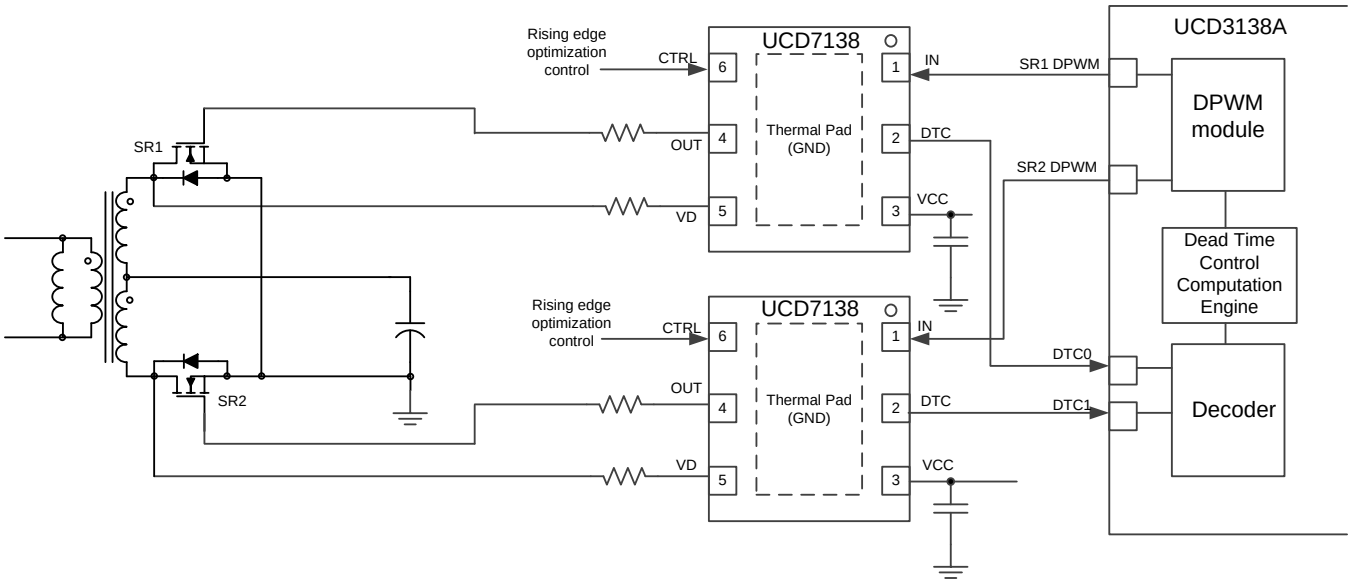

Figure 5-8. Synchronous Rectifier Peripheral use with Synchronous Rectifier Driver

DTC0 and DTC1 are received body diode conduction inputs from UCD7138. SR0_DPWM and SR1_DPWM are the DPWM waveforms for the SRs. The red and green edges are moving edges controlled by both the filter output and the DTC interface. In each cycle, right after the falling edge of the SR DPWM waveform, a body diode conduction time detection window is generated. The detection window is defined by both DETECT_BLANK and DETECT_LEN registers. During this detection window, a 4-ns timer capture counts how long the body diode conducts. Then the DPWM turn off edge of the next cycle is adjusted accordingly.

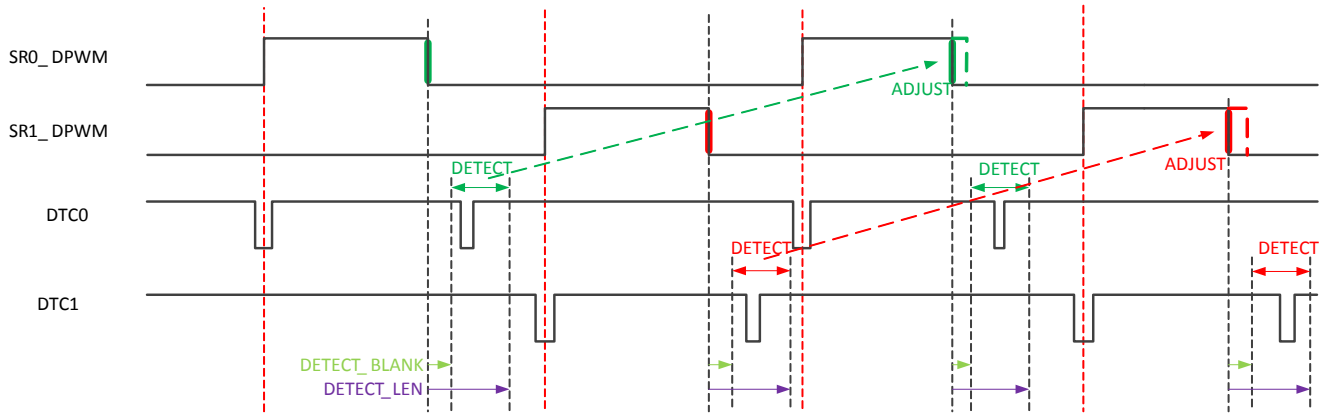

Figure 5-9. Timing Diagram of the DTC Interface

Figure 5-10 shows how the turn off edge is adjusted based on the DTC measurement of the previous cycle. The A_ADJ and B_ADJ registers in DTCMONITOR are signed accumulators; default value is 0.

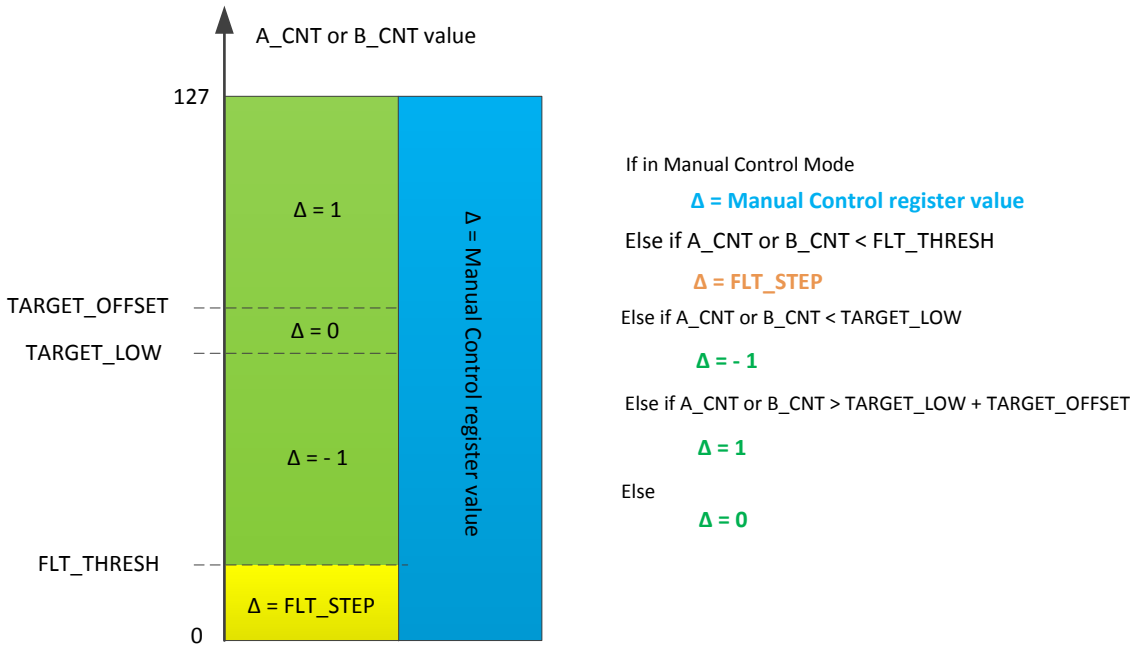

Figure 5-10. DTC Interface Principle

Based on the DTC measured, in the next cycle:

- A_ADJ = A_ADJ + A_Δ
- A_ADJ = A_ADJ + B_Δ

In each cycle, the A_ADJ and B_ADJ accumulator values are dynamically adjust the dead time. The Δ value changes after the measured body diode conduction time. A_ADJ and B_ADJ have been measured and compared to the threshold values in automatic control mode. A_ADJ and B_ADJ can be controlled by firmware while in manual control mode.

Other figures of this peripheral include negative current fault protection, consecutive fault counter, DTC input multiplexor, etc. For details, refer to the programmer's manual.

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5.9 Typical Temperature Characteristics

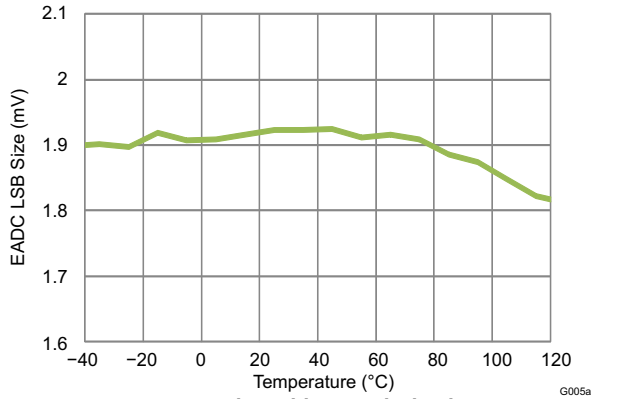

Figure 5-11. EADC LSB Size With 4X Gain (mV) vs Temperature

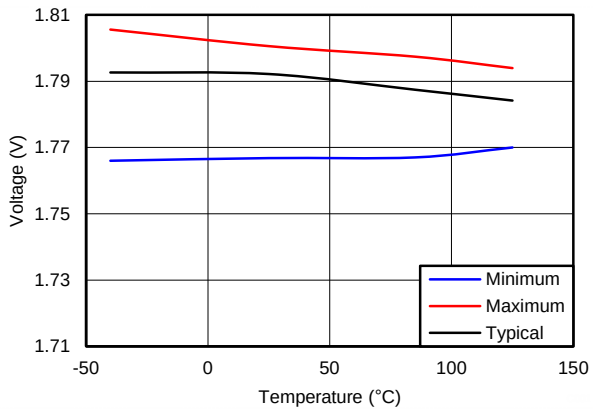

Figure 5-12. BP18 Voltage vs Temperature

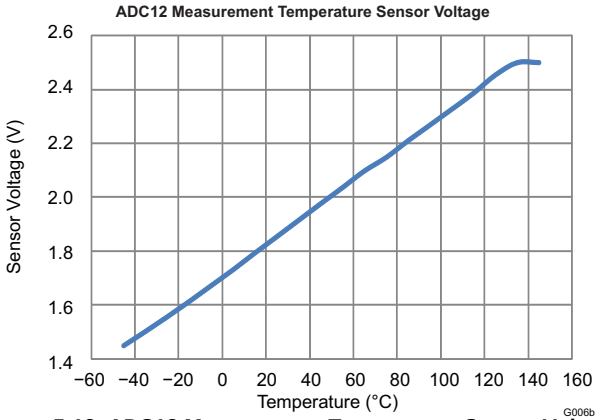

Figure 5-13. ADC12 Measurement Temperature Sensor Voltage vs Temperature

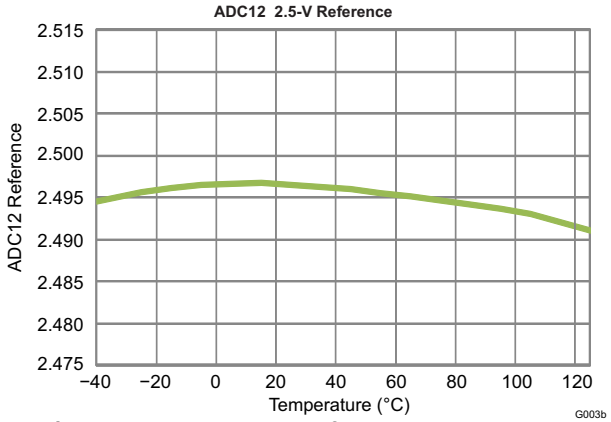

Figure 5-14. ADC12 2.5-V Reference vs Temperature

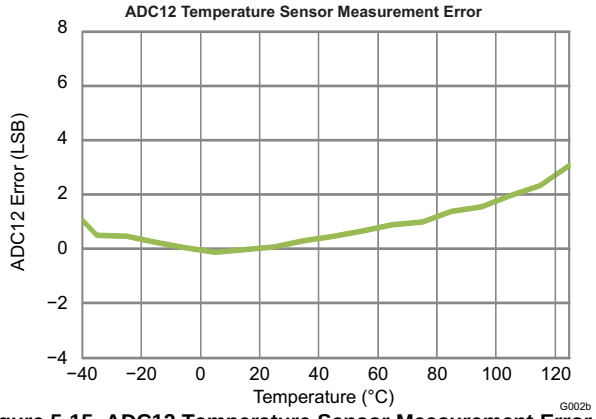

Figure 5-15. ADC12 Temperature Sensor Measurement Error vs Temperature

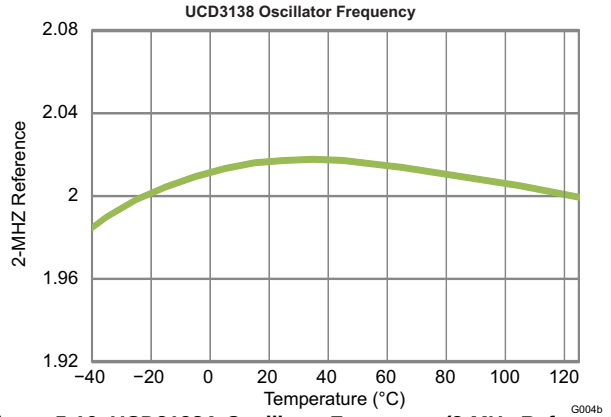

Figure 5-16. UCD3138A Oscillator Frequency (2-MHz Reference, Divided Down from 250 MHz) vs Temperature

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6 Detailed Description

6.1 Overview

The UCD3138A family is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single chip solution. The UCD3138, in comparison to Texas Instruments UCD3138A digital power controller offers 32 kB of program Flash memory. The flexible nature of the UCD3138A family makes it suitable for a wide variety of power conversion applications.

In addition, multiple peripherals inside the device have been specifically optimized to enhance the performance of AC/DC and isolated DC/DC applications and reduce the solution component count in the IT and network infrastructure space. The UCD3138A family is a fully programmable solution offering customers complete control of their application, along with ample ability to differentiate their solution. At the same time, TI is committed to simplifying our customer's development effort through offering best in class development tools, including application firmware, Code Composer StudioTM software development environment, and TI's Fusion Power Development GUI which enables customers to configure and monitor key system parameters.

6.2 ARM Processor

The ARM7TDMI-S processor is a synthesizable member of the ARM family of general purpose 32-bit microprocessors. The ARM architecture is based on RISC (Reduced Instruction Set Computer) principles where two instruction sets are available. The 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb instruction allows for higher code density equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-staged pipelined ARM processor has fetch, decode and execute stage architecture. Major blocks in the ARM processor include a 32-bit ALU, 32 x 8 multiplier, and a barrel shifter.

6.3 Memory

The UCD3138A (ARM7TDMI-S) is a Von-Neumann architecture, where a single bus provides access to all of the memory modules. All of the memory module addresses are sequentially aligned along the same address range. This applies to program flash, data flash, ROM and all other peripherals.

Within the UCD3138A architecture, there is a Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written. If a valid program is present, the ROM code branches to the main FLASH-program execution.

UCD3138A also supports customization of the boot program by allowing an alternative boot routine to be executed from program FLASH. This feature enables assignment of a unique address to each device; therefore, enabling firmware reprogramming even when several devices are connected on the same communication bus.

Two separate FLASH memory areas are present inside the device. The 32 kB Program FLASH is organized as an 8 k x 32 bit memory block and is intended to be for the firmware program. The block is configured with page erase capability for erasing blocks as small as 1kB per page, or with a mass erase for erasing the entire program FLASH array. The FLASH endurance is specified at 1000 erase/write cycles and the data retention is good for 100 years. The 2 kB data FLASH array is organized as a 512 x 32 bit memory (32 byte page size). The Data FLASH is intended for firmware data value storage and data logging. Thus, the Data FLASH is specified as a high endurance memory of 20 k cycles with embedded error correction code (ECC).

For run time data storage and scratchpad memory, a 4 kB RAM is available. The RAM is organized as a 1 k x 32 bit array.

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6.3.1 CPU Memory Map and Interrupts

When the device comes out of power-on-reset, the data memories are mapped to the processor as follows:

6.3.1.1 Memory Map (After Reset Operation)

Address	Size	Module
0x0000_0000 – 0x0000_FFFF In 16 repeated blocks of 4K each	16 X 4K	Boot ROM
0x0001_0000 – 0x0001_7FFF	32K	Program flash
0x0001_8800 – 0x0001_8FFF	2K	Data flash
0x0001_9000 – 0x0001_9FFF	4K	Data RAM

6.3.1.2 Memory Map (Normal Operation)

Just before the boot ROM program gives control to FLASH program, the ROM configures the memory as follows:

Address	Size	Module
0x0000_0000 – 0x0000_7FFF	32K	Program flash
0x0001_0000 – 0x0001_AFFF	4K	Boot ROM
0x0001_8800 – 0x0001_8FFF	2K	Data flash
0x0001_9000 – 0x0001_9FFF	4K	Data RAM

6.3.1.3 Memory Map (System and Peripherals Blocks)

Address	Size	Module
0x0002_0000 - 0x0002_00FF	256	Loop Mux
0x0003_0000 - 0x0003_00FF	256	Fault Mux
0x0004_0000 - 0x0004_00FF	256	ADC
0x0005_0000 - 0x0005_00FF	256	DPWM 3
0x0006_0000 - 0x0006_00FF	256	Filter 2
0x0007_0000 - 0x0007_00FF	256	DPWM 2
0x0008_0000 - 0x0008_00FF	256	Front End/Ramp I/F 2
0x0009_0000 - 0x0009_00FF	256	Filter 1
0x000A_0000 - 0x000A_00FF	256	DPWM 1
0x000B_0000 – 0x000B_00FF	256	Front End/Ramp I/F 1
0x000C_0000 - 0x000C_00FF	256	Filter 0
0x000D_0000 - 0x000D_00FF	256	DPWM 0
0x000E_0000 - 0x000E_00FF	256	Front End/Ramp I/F 0
0xFFF7_EC00 - 0xFFF7_ECFF	256	UART 0
0xFFF7_ED00 - 0xFFF7_EDFF	256	UART 1
0xFFF7_F000 - 0xFFF7_F0FF	256	Miscellaneous Analog Control
0xFFF7_F600 - 0xFFF7_F6FF	256	PMBus Interface
0xFFF7_FA00 - 0xFFF7_FAFF	256	GIO
0xFFF7_FD00 - 0xFFF7_FDFF	256	Timer
0xFFFF_FD00 - 0xFFFF_FDFF	256	MMC
0xFFFF_FE00 - 0xFFFF_FEFF	256	DEC
0xFFFF_FF20 - 0xFFFF_FF37	23	CIM
0xFFFF_FF40 - 0xFFFF_FF50	16	PSA
0xFFFF_FFD0 - 0xFFFF_FFEC	28	SYS

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The registers and bit definitions inside the system and peripheral blocks are detailed in the programmer's guide for each peripheral.

6.3.2 Boot ROM

The UCD3138A incorporates a 4k boot ROM. This boot ROM includes support for:

- Program download through the PMBus
- Device initialization
- Examining and modifying registers and memory
- Verifying and executing program FLASH automatically
- Jumping to a customer defined boot program

The Boot ROM is entered automatically on device reset. It initializes the device and then performs checksums on the Program FLASH. If the first 2 kB of program FLASH has a valid checksum, the program jumps to location 0 in the Program FLASH. This permits the use of a customer boot program. If the first checksum fails, it performs a checksum on the complete 32 kB of program flash. If this is valid, it also jumps to location 0 in the program flash. This permits full automated program memory checking, when there is no need for a custom boot program.

If neither checksum is valid, the Boot ROM stays in control, and accepts commands via the PMBus interface

These functions can be used to read and write to all memory locations in the UCD3138. Typically they are used to download a program to Program Flash, and to command its execution

6.3.3 Customer Boot Program

As described above, it is possible to generate a user boot program using 2 kB or more of the program flash. This can support things which the Boot ROM does not support, including:

- Program download via UART – useful especially for applications where the UCD3138A is isolated from the host (for example, PFC)
- Encrypted download – useful for code security in field updates.

6.3.4 Flash Management

The UCD3138A offers a variety of features providing for easy prototyping and easy flash programming. At the same time, high levels of security are possible for production code, even with field updates. Standard firmware will be provided for storing multiple copies of system parameters in data flash. This is minimizes the risk of losing information if programming is interrupted.

6.4 System Module

The System Module contains the interface logic and configuration registers to control and configure all the memory, peripherals and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management unit, central interrupt unit, and clock control unit.

6.4.1 Address Decoder (DEC)

The Address Decoder generates the memory selects for the FLASH, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings. These memory selects can be configured from 1 kB to 16 MB. Power on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the ARM privilege mode for user mode protection.

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6.4.2 Memory Management Controller (MMC)

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 kB of address space decoding.

6.4.3 System Management (SYS)

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripherals modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. A clock control setup for the processor clock (MCLK) speed, is also available.

6.4.4 Central Interrupt Module (CIM)

The CIM accepts 32 interrupt requests for meeting firmware timing requirements. The ARM processor supports two interrupt levels: FIQ and IRQ. FIQ is the highest priority interrupt. The CIM provides hardware expansion of interrupts by use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest precedence channel with a pending interrupt and is used to locate the interrupt vector address from the interrupt vector table. Interrupt channel 0 has the lowest precedence and interrupt channel 31 has the highest precedence. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable, allowing individual channels to be selectively disabled or enabled.

Table 6-1. Interrupt Priority Table

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
BRN_OUT_INT	Brownout	Brownout interrupt	0 (lowest)
EXT_INT	External interrupts	Interrupt on external input pin	1
WDRST_INT	Watchdog control	Interrupt from watchdog exceeded (reset)	2
WDWAKE_INT	Watchdog control	Wakeup interrupt when watchdog equals half of set watch time	3
SCI_ERR_INT	UART or SCI control	UART or SCI error Interrupt. Frame, parity or overrun	4
SCI_RX_0_INT	UART or SCI control	UART0 RX buffer has a byte	5
SCI_TX_0_INT	UART or SCI control	UART0 TX buffer empty	6
SCI_RX_1_INT	UART or SCI control	UART1 RX buffer has a byte	7
SCI_TX_1_INT	UART or SCI control	UART1 TX buffer empty	8
PMBUS_INT		PMBus related interrupt	9
DIG_COMP_INT	12-bit ADC control	Digital comparator interrupt	10
FE0_INT	Front End 0	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	11
FE1_INT	Front End 1	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	12
FE2_INT	Front End 2	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	13
PWM3_INT	16-bit timer PWM 3	16-bit Timer PWM3 counter overflow or compare interrupt	14
PWM2_INT	16-bit timer PWM 2	16-bit Timer PWM2 counter Overflow or compare interrupt	15
PWM1_INT	16-bit timer PWM 1	16-bit Timer PWM1 counter overflow or compare interrupt	16
PWM0_INT	16-bit timer PWM 0	16-bit Timer PWM1 counter overflow or compare interrupt	17
OVF24_INT	24-bit timer control	24-bit Timer counter overflow interrupt	18
DTC_FLT_INT	DTC fault interrupt	DTC module fault interrupt	19
COMP_1_INT	24-bit timer control	24-bit Timer compare 1 interrupt	20

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Table 6-1. Interrupt Priority Table (continued)

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
CAPTURE_0_INT	24-bit timer control	24-bit Timer capture 0 interrupt	21
COMP_0_INT	24-bit timer control	24-bit Timer compare 0 interrupt	22
CPCC_INT	Constant power constant current	Mode switched in CPCC module Flag needs to be read for details	23
ADC_CONV_INT	12-bit ADC control	ADC end of conversion interrupt	24
FAULT_INT	Fault Mux interrupt	Analog comparator interrupts, overvoltage detection, undervoltage detection, LLM load step detection	25
DPWM3	DPWM3	Same as DPWM1	26
DPWM2	DPWM2	Same as DPWM1	27
DPWM1	DPWM1	1) Every (1 to 256) switching cycles 2) Fault detection 3) Mode switching	28
DPWM0	DPWM0	Same as DPWM1	29
EXT_FAULT_INT	External Faults	Fault pin interrupt	30
SYS_SSI_INT	System Software	System software interrupt	31 (highest)

6.5 DPWM Modes of Operation

The DPWM is a complex logic system which is highly configurable to support several different power supply topologies. The discussion below will focus primarily on waveforms, timing and register settings, rather than on logic design.

The DPWM is centered on a period counter, which counts up from 0 to PRD, and then is reset and starts over again.

The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.

6.5.1 Normal Mode

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful for buck topologies. The drawing of the Normal Mode waveforms is shown in Figure 6-1.

Cycle adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used for functions like current balancing. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (for an average output), or at the end of the on-time (to minimize phase delay) The Adaptive Sample Register provides an offset from the center of the on-time. This can compensate for external delays, such as MOSFET and gate driver turn on times.

Blanking A-Begin and Blanking A-End can be used to blank out noise from the MOSFET turn on at the beginning of the period (DPWMA rising edge). Blanking B could be used at the turn off time of DPWMB. The other edges are dynamic, so blanking is more difficult.

Cycle Adjust B has no effect in Normal Mode.

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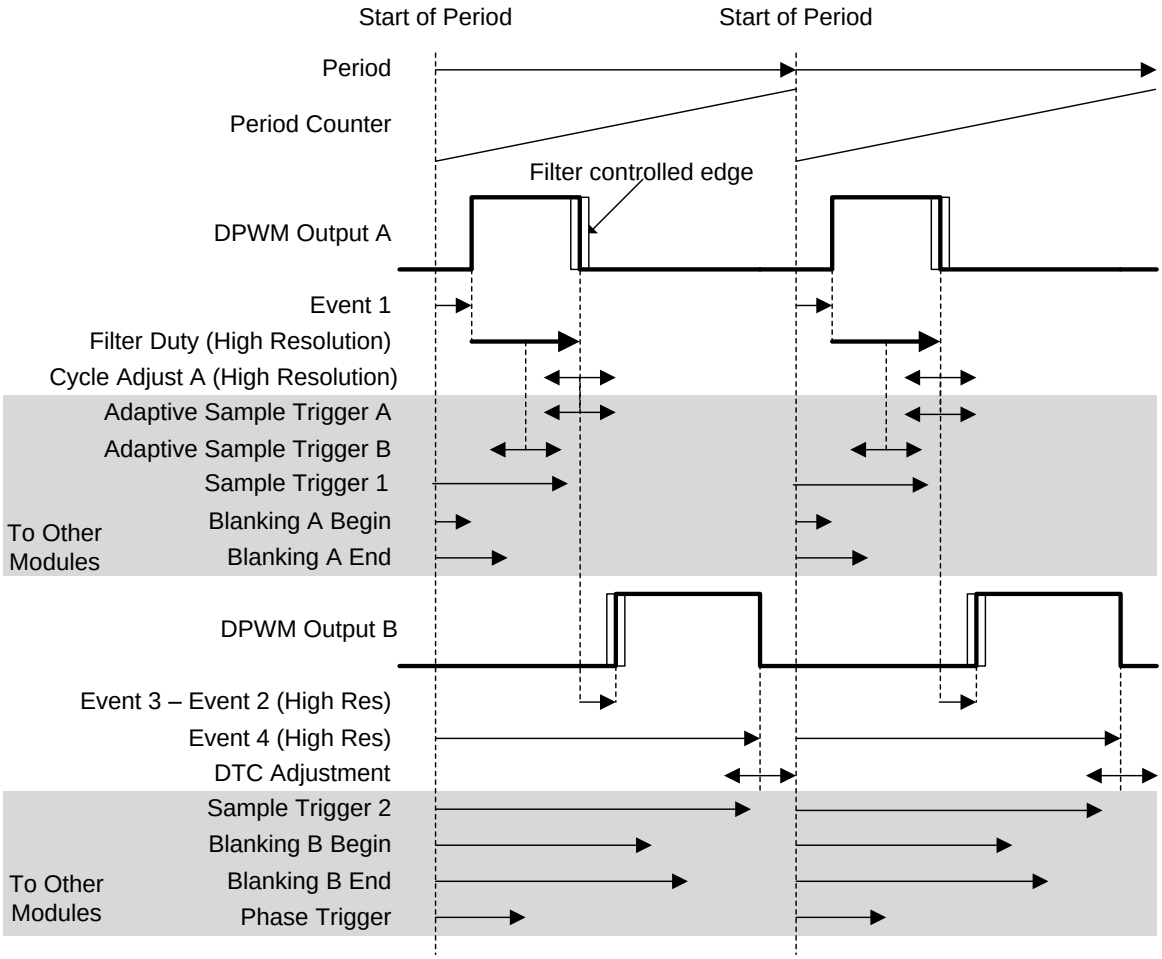

Events which change with DPWM mode:

- DPWM A Rising Edge = Event 1
- DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A
- Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
- Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
- DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)
- DPWM B Falling Edge = Event 4 + DTC Adjustment
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 6-1. Normal Mode Closed Loop

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6.5.2 DPWM Multiple Output Mode

Multi mode is used for systems where each phase has only one driver signal. It enables each DPWM peripheral to drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

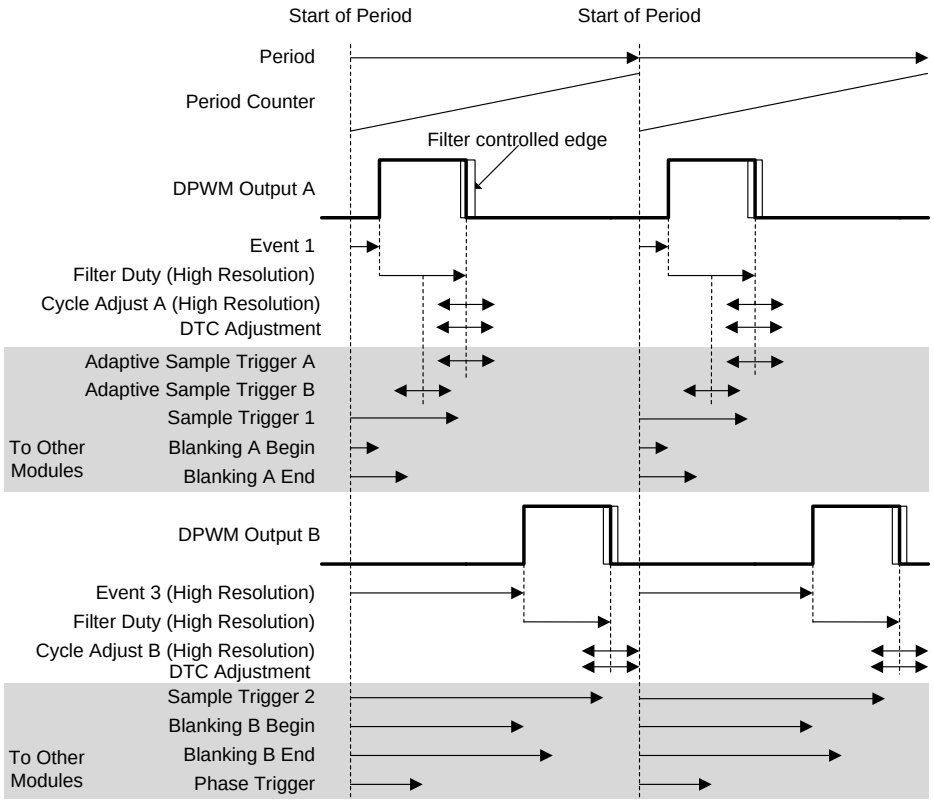
The diagram for Multi-Mode is shown in Figure 6-2.

Event 2 and Event 4 are not relevant in Multi mode.

DPWMB can cross over the period boundary safely, and still have the proper pulse width, so full 100% pulse width operation is possible. DPWMA cannot cross over the period boundary.

Since the rising edge on DPWM B is also fixed, Blanking B-Begin and Blanking B-End can be used for blanking this rising edge.

Cycle Adjust B is usable on DPWM B.



Events which change with DPWM mode:

- DPWM A Rising Edge = Event 1
- DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A + DTC Adjustment
- Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
- Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
- DPWM B Rising Edge = Event 3
- DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B + DTC Adjustment
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 6-2. Multi Mode Closed Loop

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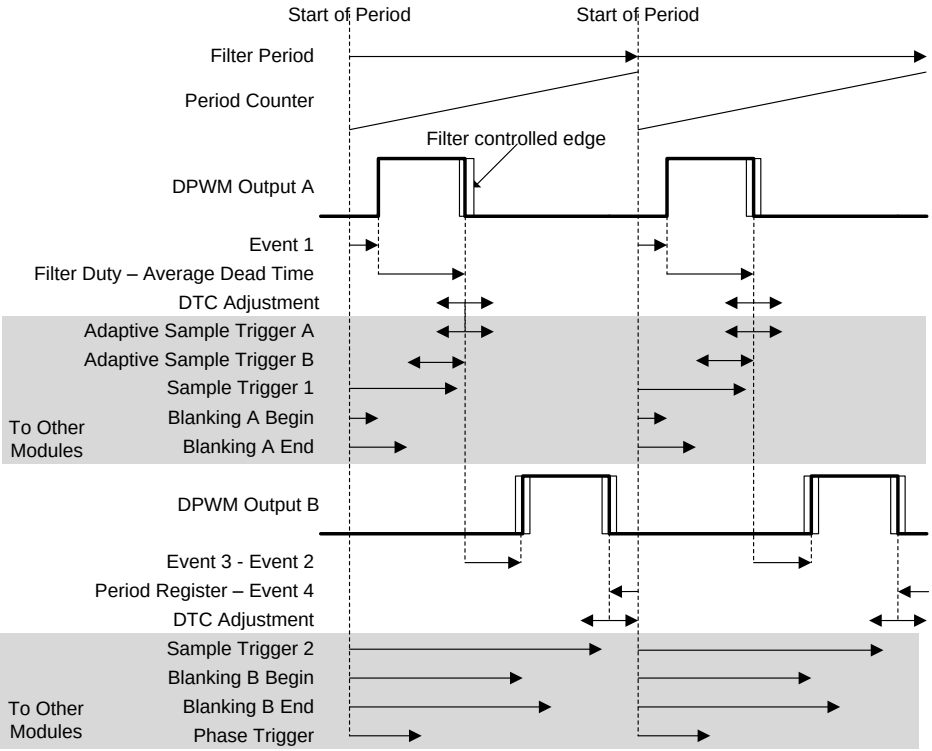
6.5.3 DPWM Resonant Mode

This mode provides a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same.

The equations for this mode are designed for a smooth transition from PWM mode to resonant mode, as described in *Section 6.7.2*. The diagram of this mode is shown in Figure 6-3.

The Filter has two outputs, Filter Duty and Filter Period. In this case, the Filter is configured so that the Filter Period is twice the Filter Duty. So if there were no dead times, each DPWM pin would be on for half of the period. For dead time handling, the average of the two dead times is subtracted from the Filter Duty for both DPWM pins. Therefore, both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. This is the only edge for which the blanking signals can be used easily.



Events which change with DPWM mode:

- Dead Time 1 = Event 3 - Event 2
- Dead Time 2 = Event 1 + Period Register - Event 4
- Average Dead Time = (Dead Time 1 + Dead Time 2)/2

- DPWM A Rising Edge = Event 1
- DPWM A Falling Edge = Event 1 + Filter Duty - Average Dead Time + DTC Adjustment
- Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or
- Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register
- DPWM B Rising Edge = Event 1 + Filter Duty - Average Dead Time + (Event 3 - Event 2)
- DPWM B Falling Edge = Filter Period - (Period Register - Event 4) + DTC Adjustment
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 6-3. Resonant Symmetrical Closed Loop

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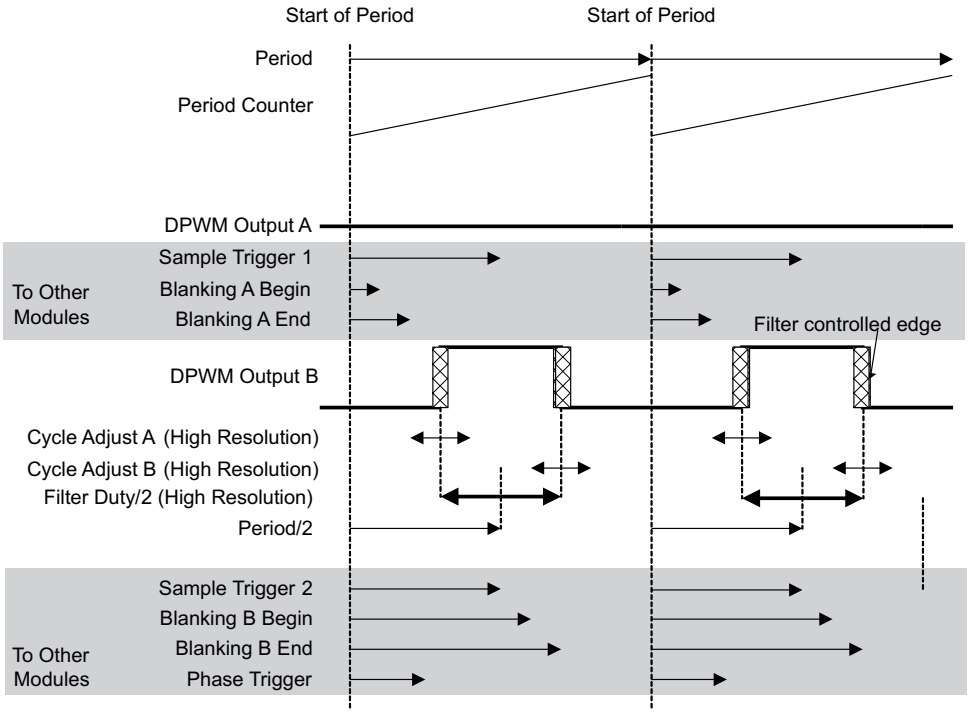
6.5.4 Triangular Mode

Triangular mode provides a stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM-B is available. The diagram for Triangular Mode is shown in Figure 6-4.

All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the FET on-time, because the center of the on-time does not move in this mode.



Events which change with DPWM mode:

- DPWM A Rising Edge = None
- DPWM A Falling Edge = None
- Adaptive Sample Trigger = None
- DPWM B Rising Edge = Period / 2 - Filter Duty / 2 + Cycle Adjust A
- DPWM B Falling Edge = Period / 2 + Filter Duty / 2 + Cycle Adjust B
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 6-4. Triangular Mode Closed Loop

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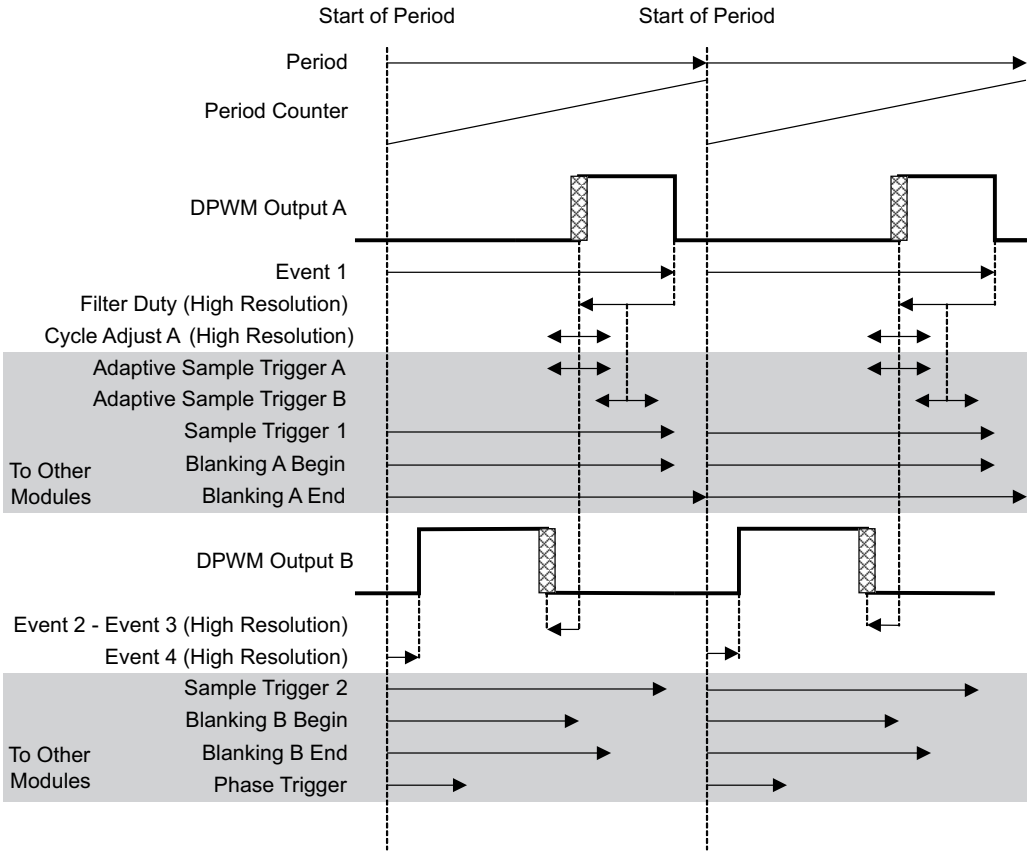
6.5.5 Leading Edge Mode

Leading edge mode is very similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWM B falling edge stays ahead of the DPWMA rising edge by a fixed dead time. The diagram of the Leading Edge Mode is shown in Figure 6-5.

As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.



Events which change with DPWM mode:

- DPWM A Rising Edge = Event 1
- DPWM A Falling Edge = = Event 1 - Filter Duty + Cycle Adjust A
- Adaptive Sample Trigger A = Event 1 - Filter Duty + Adaptive Sample Register or
- Adaptive Sample Trigger B = Event 1 - Filter Duty / 2 + Adaptive Sample Register
- DPWM B Rising Edge = Event 4
- DPWM B Falling Edge = Event 1 - Filter Duty + Cycle Adjust A - (Event 2 – Event 3)
- Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

- Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B
- Begin, Blanking B End

Figure 6-5. Leading Edge Closed Loop

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6.6 Sync FET Ramp and IDE Calculation

The UCD3138A has built in logic for controlling MOSFETs for synchronous rectification (Sync FETs). This comes in two forms:

- Sync FET ramp
- Ideal Diode Emulation (IDE) calculation

When starting up a power supply, sometimes there is already a voltage on the output – this is called prebias. It is difficult to calculate the ideal Sync FET on-time for this case. If it is not calculated correctly, it may pull down the prebias voltage, causing the power supply to sink current.

To avoid this, Sync FETs are not turned on until the power supply has ramped up to the nominal voltage. The Sync FETs are turned on gradually in order to avoid an output voltage glitch. The Sync FET Ramp logic can be used to turn them on at a rate below the bandwidth of the filter.

In discontinuous mode, the ideal on-time for the Sync FETs is a function of V_{IN}, V_{OUT}, and the primary side duty cycle (D). The IDE logic in the UCD3138A takes V_{IN} and V_{OUT} data from the firmware and combines it with D data from the filter hardware. It uses this information to calculate the ideal on-time for the Sync FETs.

6.7 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically. This is useful to increase efficiency and power range. The following paragraphs describe phase-shifted full bridge and LLC examples:

6.7.1 Phase Shifted Full Bridge Example

Phase shifted full bridge topologies are shown in Figure 6-6 and Figure 6-7.

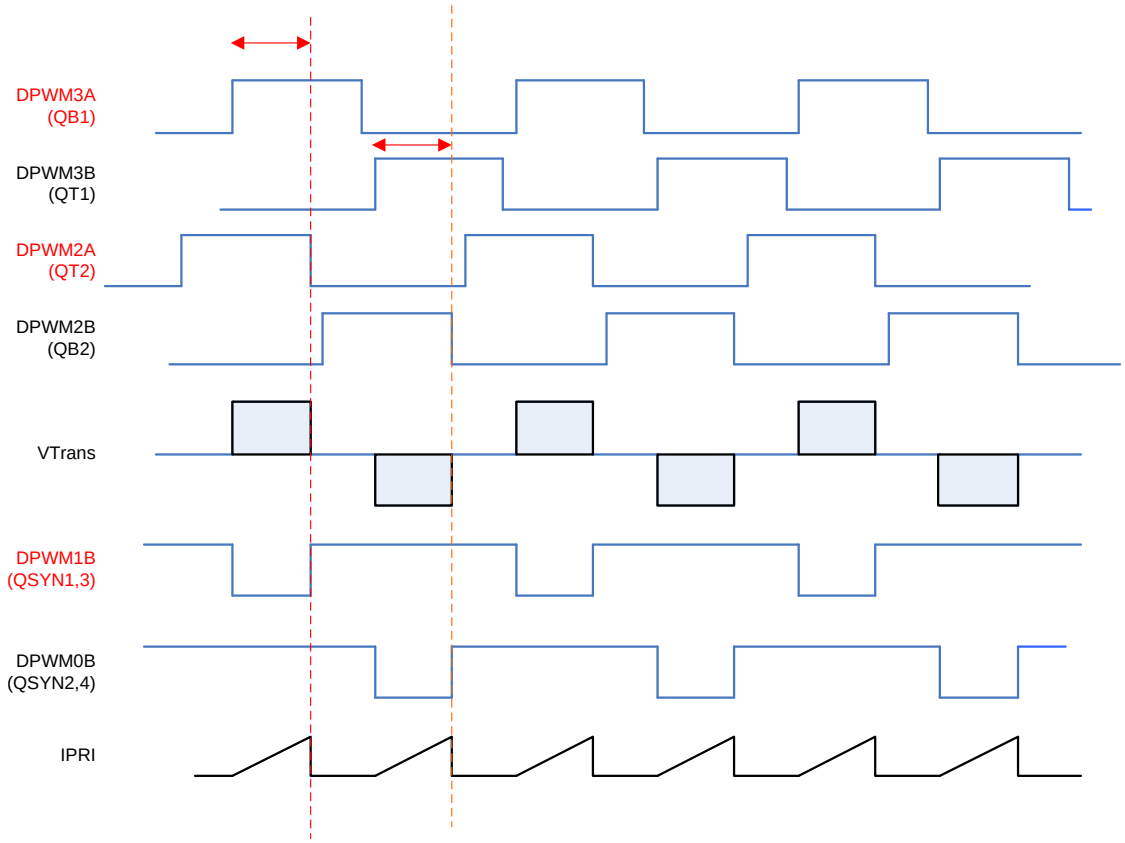

Figure 6-6. Phase Shifted Full Bridge

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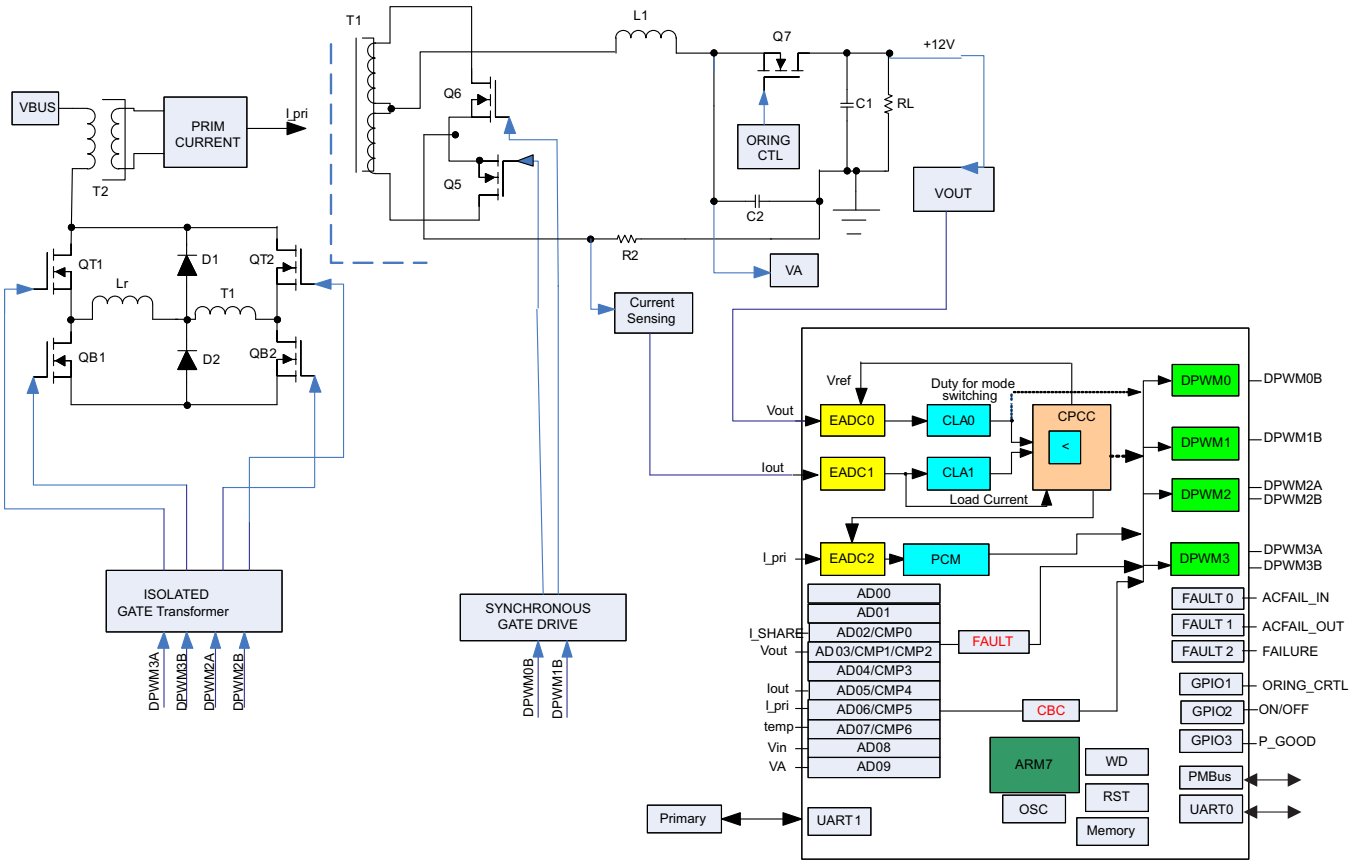
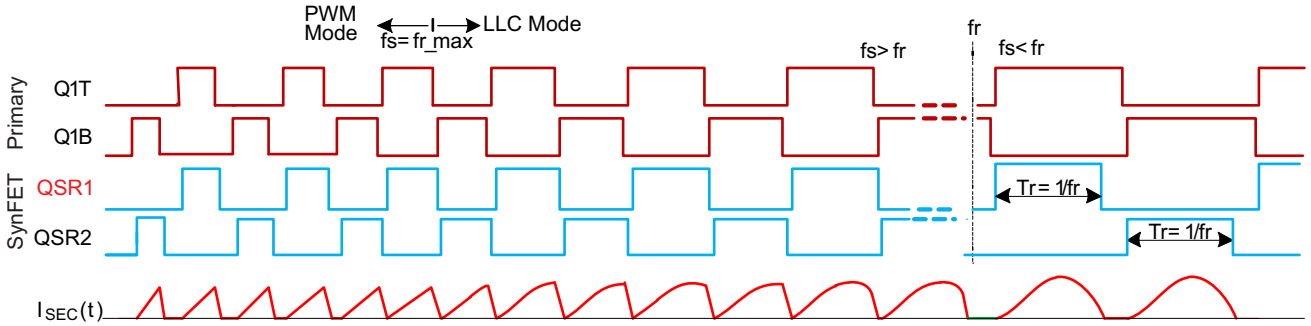


Figure 6-7. Secondary-Referenced Phase-Shifted Full Bridge Control With Synchronous Rectification

6.7.2 LLC Example

In LLC, three modes are used. At the highest frequency, a pulse width modulated mode (Multi Mode) is used. As the frequency decreases, resonant mode is used. As the frequency gets still lower, the synchronous MOSFET drive changes so that the on-time is fixed and does not increase. In addition, the LLC control supports cycle-by-cycle current limiting. This protection function operates by a comparator monitoring the maximum current during the DPWMA conduction time. Any time this current exceeds the programmable comparator reference the pulse is immediately terminated. Due to classic instability issues associated with half-bridge topologies it is also possible to force DPWMB to match the truncated pulse width of DPWMA. Here are the waveforms for the LLC:



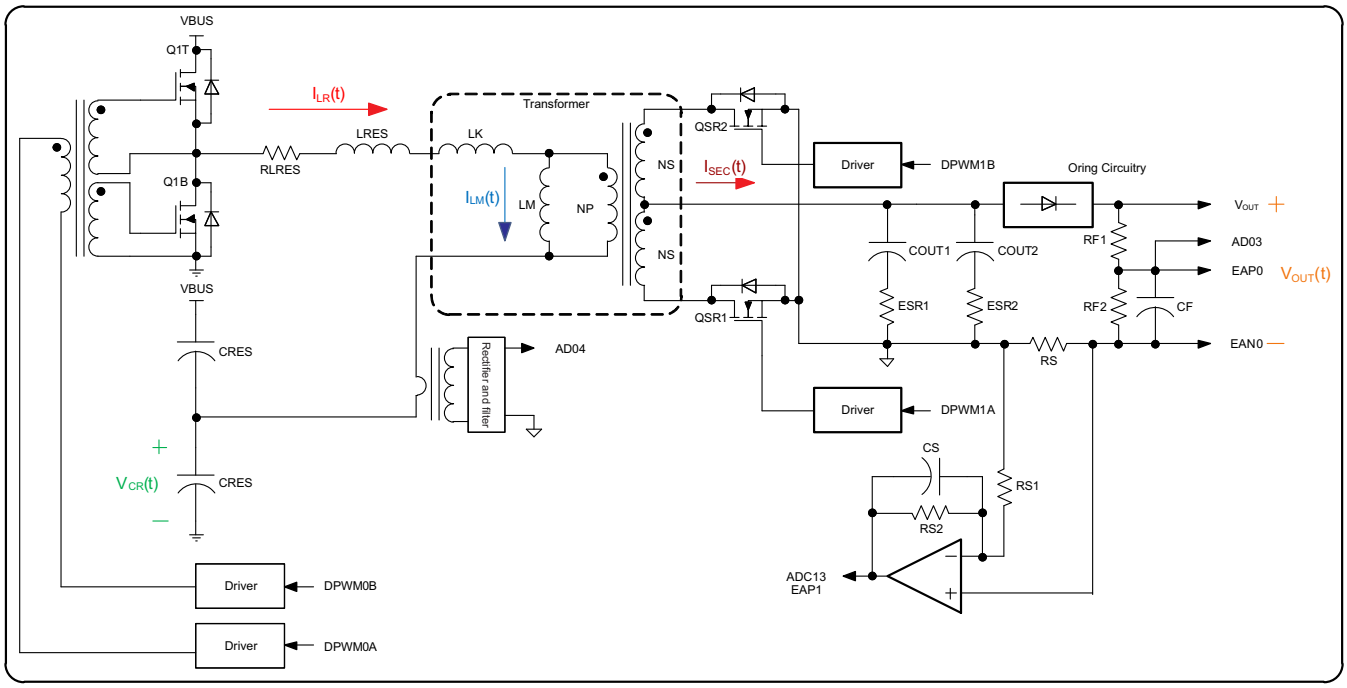


Figure 6-8. Secondary-Referenced Half-Bridge Resonant LLC Control With Synchronous Rectification

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6.7.3 Mechanism for Automatic Mode Switching

The UCD3138A allows the customer to enable up to two distinct levels of automatic mode switching. These different modes are used to enhance light load operation, short circuit operation and soft start. Many of the configuration parameters for the DPWM are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the filter duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown in Figure 6-9.

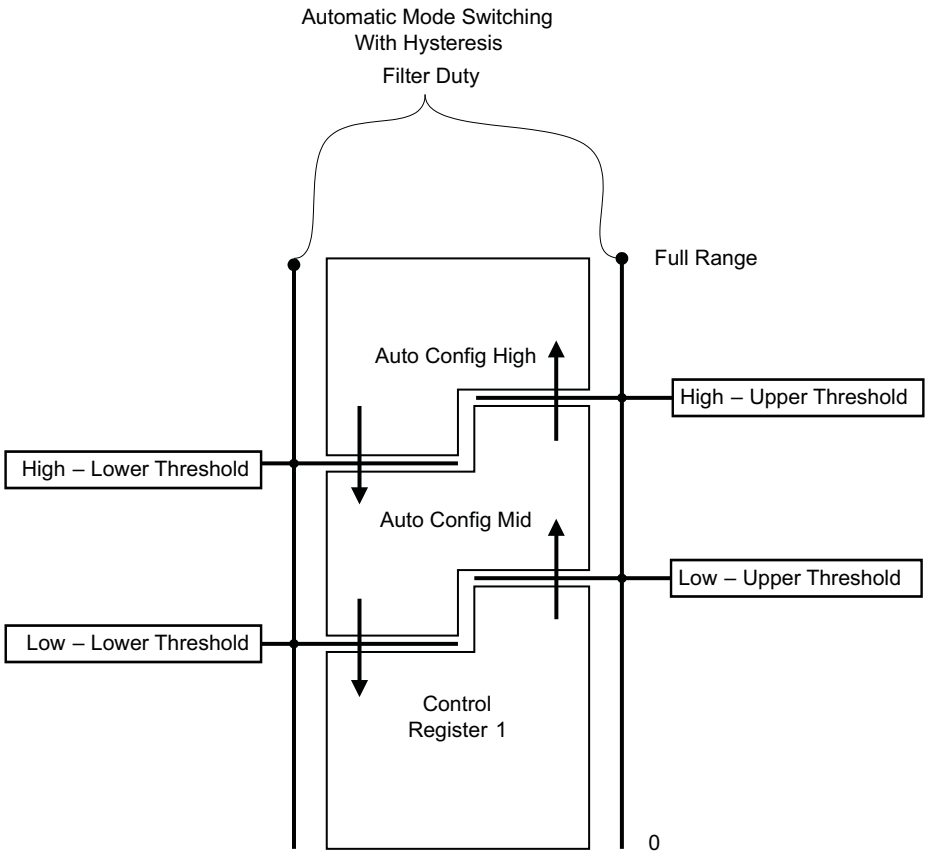

Figure 6-9. Automatic Mode Switching

As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Auto Config Mid until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point.

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6.8 DPWMC, Edge Generation, IntraMux

The UCD3138A has hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed – DPWMC, the Edge Generation Module, and the IntraMux.

DPWMC is an auxillary signal inside the DPWM logic. It can be generated using the Blanking A begin time, and the Blanking A end time.

The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can output a generated edge.

The options are:

0 = DPWM(n) A Rising edge
1 = DPWM(n) A Falling edge
2 = DPWM(n) B Rising edge
3 = DPWM(n) B Falling edge
4 = DPWM(n+1) A Rising edge
5 = DPWM(n+1) A Falling edge
6 = DPWM(n+1) B Rising edge
7 = DPWM(n+1) B Falling edge

Where “n" is the numerical index of the DPWM module of interest. For example n=1 refers to DPWM1.

The Edge Gen is controlled by the DPWMEDGEGEN register.

The IntraMux (short for intra multiplexer) is controlled by the Auto Config registers. The IntraMux takes signals from multiple DPWMs and from the Edge Gen and combines them logically to generate DPWMA and DPWMB signals This is useful for topologies like phase-shifted full bridge, especially when they are controlled with automatic mode switching. Of course, it can all be disabled, and DPWMA and DPWMB will be driven as described in the sections above. If the Intra Mux is enabled, high resolution must be disabled, and DPWM edge resolution goes down to 4 ns.

The Edge Gen/Intra Mux is shown in Figure 6-10.

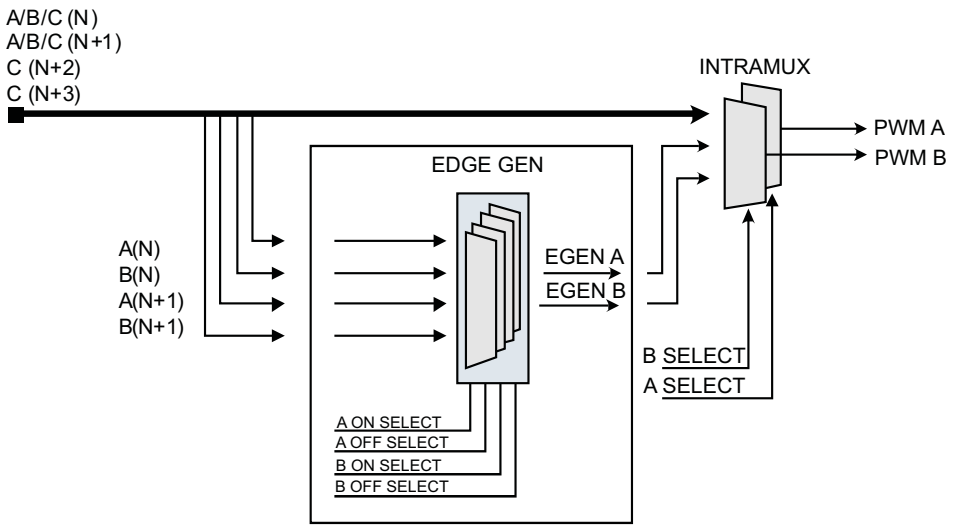

Figure 6-10. Edge Gen/Intra Mux

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A list of the IntraMux modes for DPWMA is as follows:

0 = DPWMA(n) pass through (default)
1 = Edge-gen output, DPWMA(n)
2 = DPWNC(n)
3 = DPWMB(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

and for DPWMB:

0 = DPWMB(n) pass through (default)
1 = Edge-gen output, DPWMB(n)
2 = DPWNC(n)
3 = DPWMA(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM3 the following definitions apply:

DPWM(n)	DPWM3
DPWM(n+1)	DPWM0
DPWM(n+2)	DPWM1
DPWM(n+3)	DPWM2

6.9 Filter

The UCD3138A filter is a PID filter with many enhancements for power supply control. Some of its features include:

- Traditional PID Architecture
- Programmable non-linear limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout filter calculations
- Programmable clamps on integrator branch and filter output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to turn off calculations on any of the individual filter branches
- Duty cycle, resonant period, or phase shift generation based on filter output.
- Flux balancing
- Voltage feed forward

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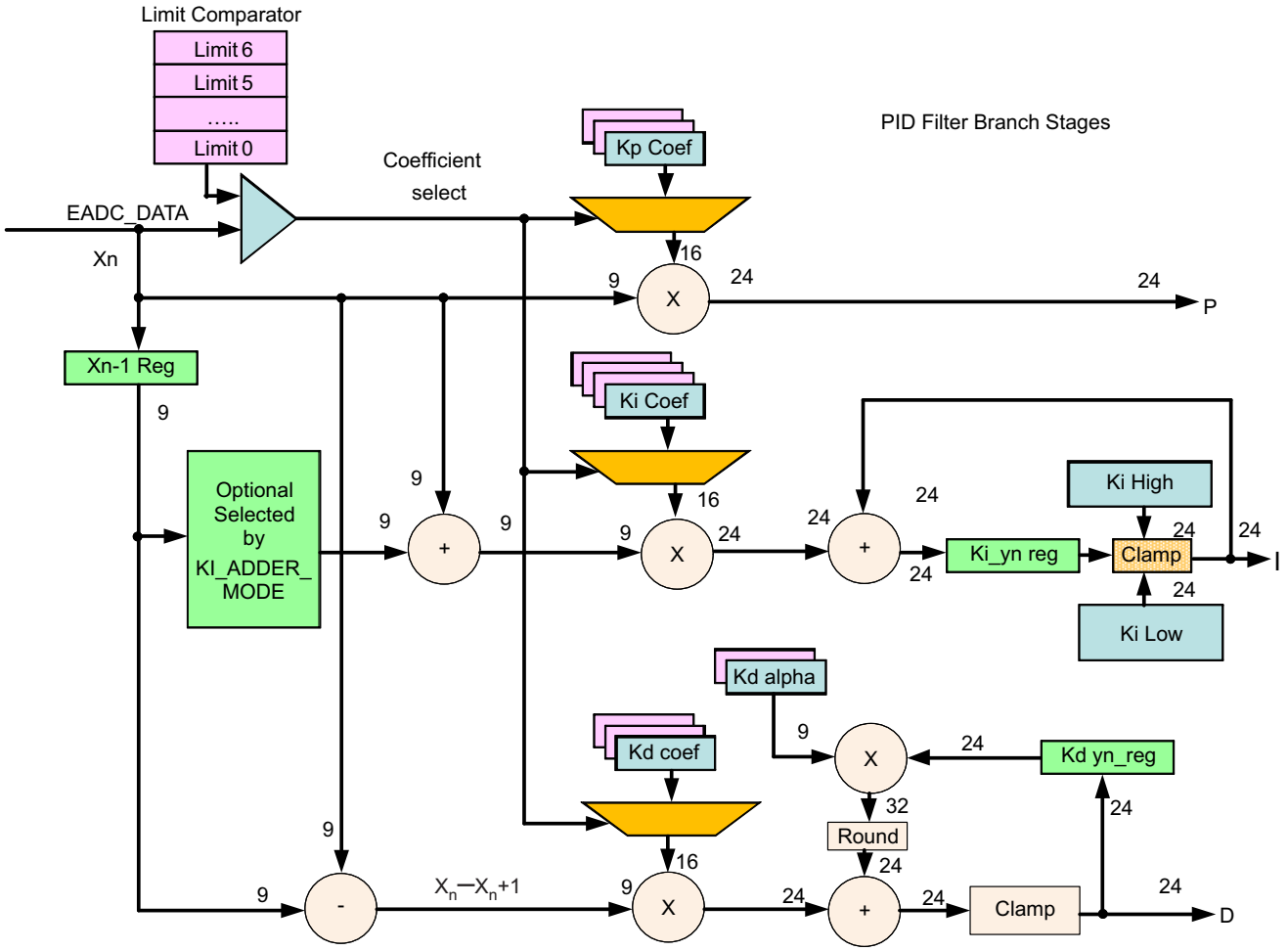

Figure 6-11. First Section of the Filter

The filter input, Xn, generally comes from a front end. Then there are three branches, P, I. and D. Note that the D branch also has a pole, Kd Alpha. Clamps are provided both on the I branch and on the D alpha pole.

The filter also supports a nonlinear mode, where up to 7 different sets of coefficients can be selected depending on the magnitude of the error input Xn. This can be used to increase the filter gain for higher errors to improve transient response.

Tthe output section of the filter (S0.23 means that there is 1 sign bit, 0 integer bits and 23 fractional bits) is shown in Figure 6-12

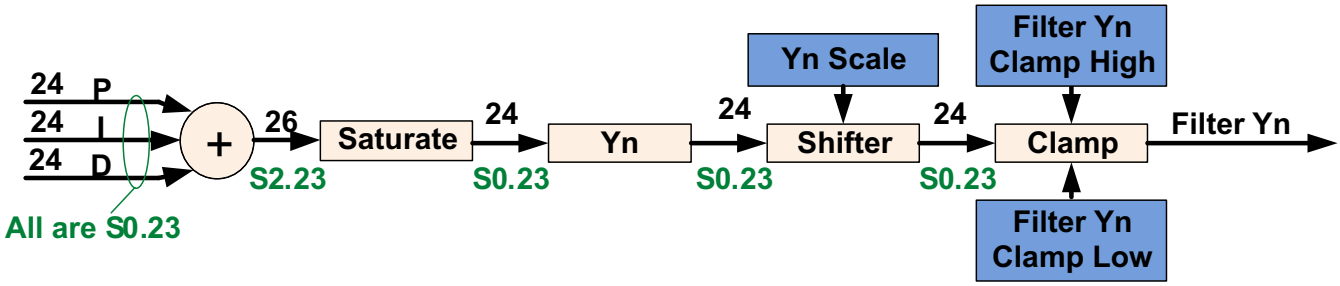

Figure 6-12. Output Section of the Filter

This section combines the P, I, and D sections, and provides for saturation, scaling, and clamping.

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The final section for the filter, which permits its output to be matched to the DPWM is shown in Figure 6-13.

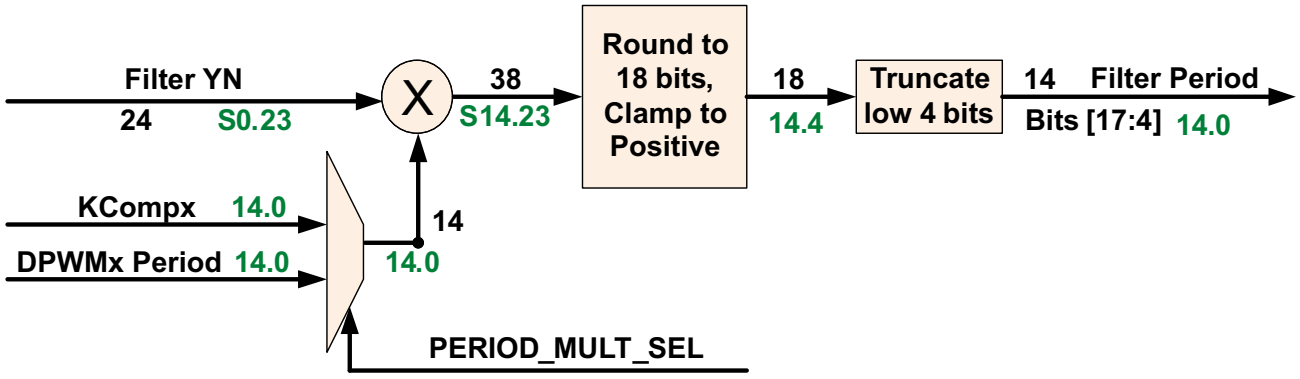

Figure 6-13. Final Section for the Filter

This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

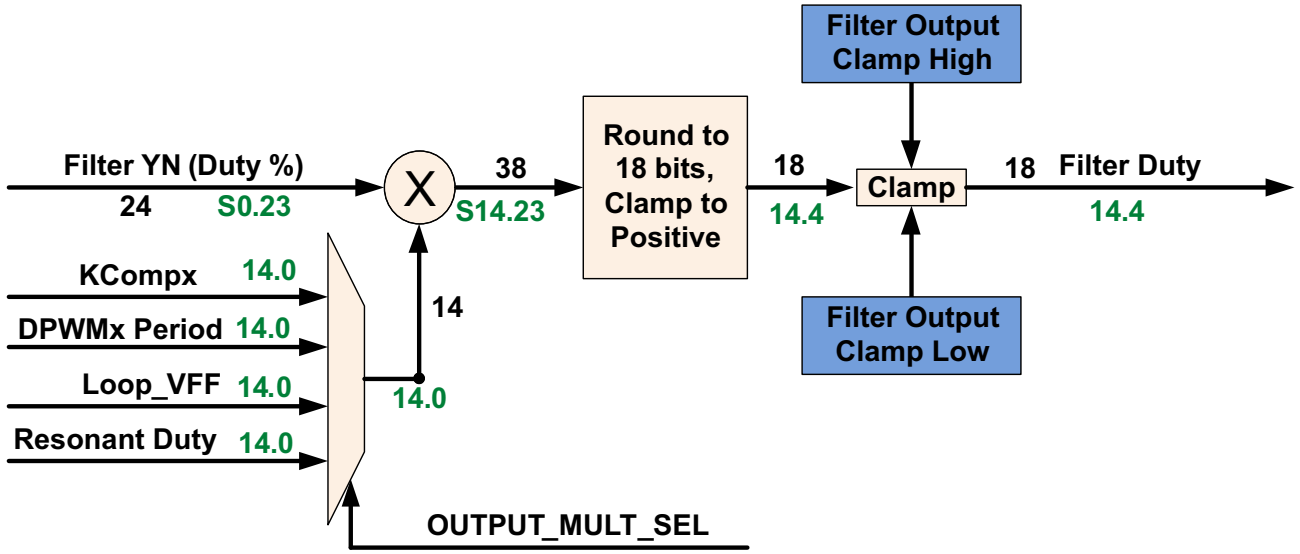

Figure 6-14. Resonant Mode

6.9.1 Loop Multiplexer

The Loop Mux controls interconnections between the filters, front ends, and DPWMs. Any filter, front end, and DPWM can be combined with each other in many configurations.

It also controls the following connections:

- DPWM to Front End
- Front End DAC control from Filters or Constant Current/Constant Power Module
- Filter Special Coefficients and Feed Forward
- DPWM synchronization
- Filter to DPWM

The following control modules are configured in the Loop Mux:

- Constant Power/Constant Current

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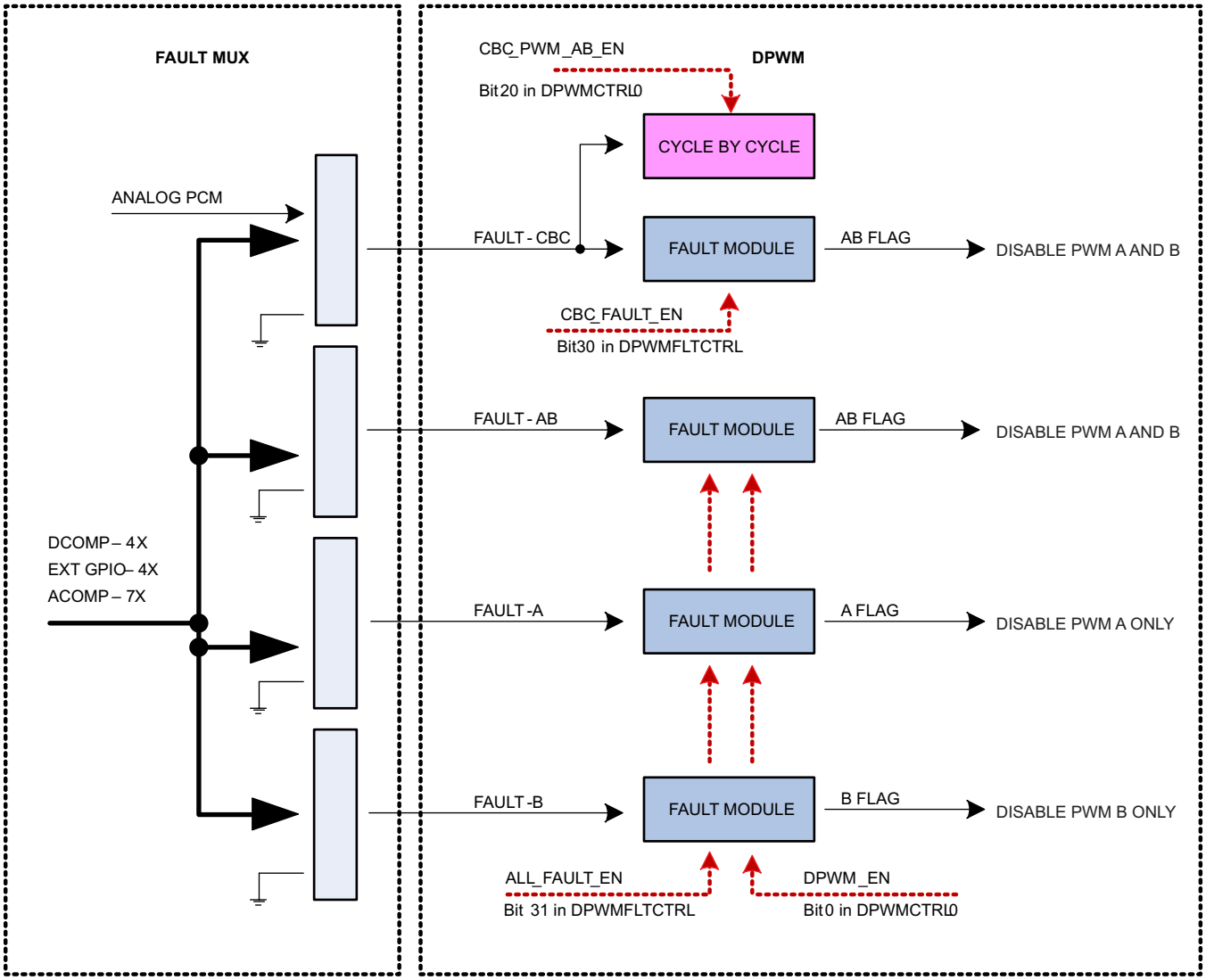
- Cycle Adjustment (Current and flux balancing)
- Global Period
- Light Load (Burst Mode)
- Analog Peak Current Mode

6.9.2 Fault Multiplexer

In order to allow a flexible way of mapping several fault triggering sources to all the DPWMs channels, the UCD3138A provides an extensive array of multiplexers that are united under the name Fault Mux module.

The Fault Mux Module supports flexible mapping between fault sources and fault response mechanism inside each DPWM module.

- Many fault sources can be mapped to a single fault response mechanism. For instance an analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a fault-A signal connected to a single FAULT MODULE and shut down DPWM1-A.
- A single fault source can be mapped to many fault response mechanisms inside many DPWM modules. For instance an analog comparator in charge of over current protection can be mapped to DPWM-0 through DPWM-3 by way of several fault modules.



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The Fault Mux Module provides a multitude of fault protection functions within the UCD3138A high-speed loop (front end control, filter, DPWM and loop Mux modules). The Fault Mux Module allows highly configurable fault generation based on digital comparators, high-speed analog comparators and external fault pins. Each of the fault inputs to the DPWM modules can be configured to one or any combination of the fault events provided in the Fault Mux Module.

Each one of the DPWM engines has four fault modules. The modules are called CBC fault module, AB fault module, A fault module and B fault module.

The internal circuitry in all the four fault modules is identical, and the difference between the modules is limited to the output it affects under a fault condition.

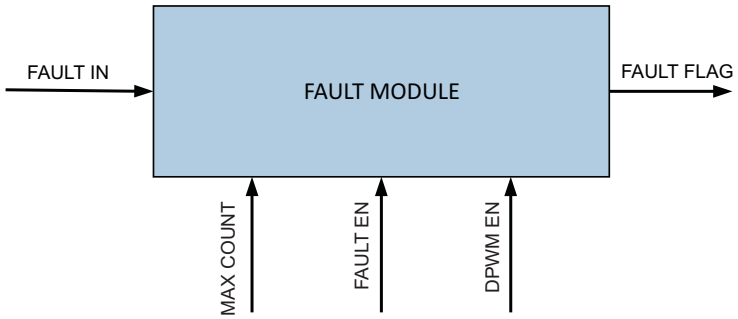

Figure 6-15. Fault Module

All fault modules are capable of detecting faults only once per DPWM switching cycle. Each one of the fault modules have a separate max_count and the fault flag will be set only if sequential faults count exceeds max_count.

Once the fault flag is set DPWMs need to be disabled by DPWM_EN going low in order to clear the fault flags. Note, all four Fault Modules share the same DPWM_EN control, all fault flags (output of Fault Modules) is cleared simultaneously.

All four Fault Modules share the same global FAULT_EN as well. Therefore, a specific Fault Module cannot be enabled/ disabled separately.

Figure 6-16. Cycle by Cycle Block

In contrast to the fault modules, only one cycle by cycle block is available in each DPWM module.

The cycle by cycle block can work in conjunction with CBC Fault Module and enables DPWM reaction to signals arriving from analog peak current mode (PCM) module.

The fault Mux module supports the following basic functions:

- 4 digital comparators with programmable thresholds and fault generation
- Configuration for 7 high-speed analog comparators with programmable thresholds and fault generation
- External GPIO detection control with programmable fault generation
- Configurable DPWM fault generation for DPWM current limit fault, DPWM overvoltage detection fault, DPWM A external fault, DPWM B external fault and DPWM IDE flag
- Clock failure detection for high and low frequency oscillator blocks
- Discontinuous conduction mode detection

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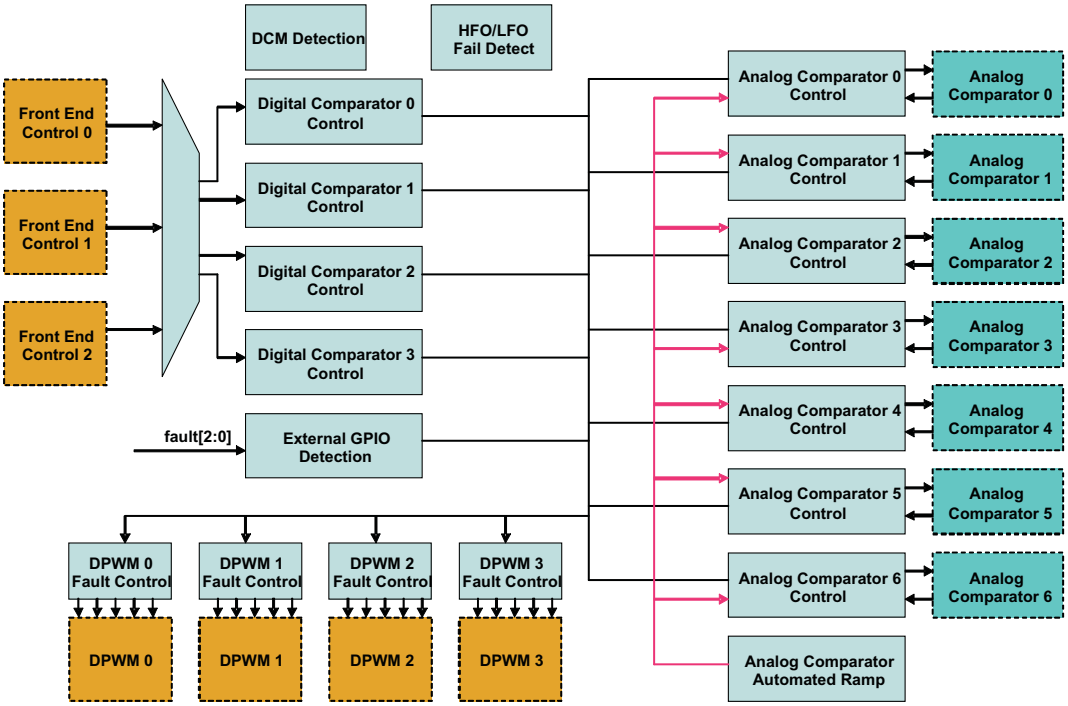

Figure 6-17. Fault Mux Block Diagram

6.10 Communication Ports

6.10.1 SCI (UART) Serial Communication Interface

A maximum of two independent Serial Communication Interface (SCI) or Universal Asynchronous Receiver/Transmitter pre-scaler (UART) interfaces are included within the device for asynchronous start-stop serial data communication (see the pin out sections for details) Each interface has a 24 bit for supporting programmable baud rates and has programmable data word and stop bit options. Half or full duplex operation is configurable through register bits. A loop back feature can also be setup for firmware verification. Both SCI-TX and SCI-RX pin sets can be used as GPIO pins when the peripheral is not being used. Both the UART ports support Hardware auto baud correction improving robustness in communication even at higher baud rates.

6.10.2 PMBUS

The PMBus Interface supports independent master and slave modes controlled directly by firmware through a processor bus interface. Individual control and status registers enable firmware to send or receive I2C, SMBus or PMBus messages in any of the accepted protocols, in accordance with the I^2C Specification, SMBus Specification (Version 2.0) and the PMBUS Power System Management Protocol Specification (PMBus 1.3).

The PMBus interface is controlled through a processor bus interface, utilizing a 32-bit data bus and 6-bit address bus. The PMBus interface is connected to the expansion bus, which features 4 byte write enables, a peripheral select dedicated for the PMBus interface, separated 32-bit data buses for reading and writing of data and active-low write and output enable control signals. In addition, the PMBus Interface connects directly to the I^2C/SMBus/PMBus Clock, Data, Alert, and Control signals.

Example: PMBus Address Decode via ADC12 Reading

The user can allocate 2 pins of the 12-bit ADC input channels, AD_00 and AD_01, for PMBus address decoding. At power-up the device applies I_{BIAS} to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC.

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Where bin(V_{AD0x}) is the address bin for one of 12 address as shown in Figure 6-18.

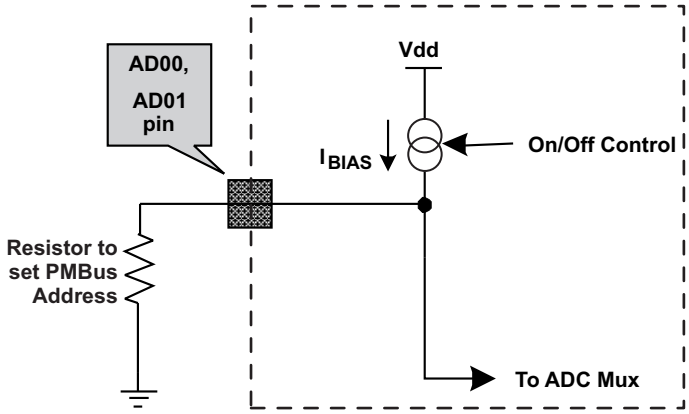

Figure 6-18. PMBus Address Detection Method

6.10.3 General Purpose ADC12

The ADC12 is a 12 bit, high speed analog to digital converter, equipped with the following options:

- Typical conversion speed of 267 ksps
- Conversions can consist from 1 to 16 ADC channel conversions in any desired sequence
- Post conversion averaging capability, ranging from 4X, 8X, 16X or 32X samples
- Configurable triggering for ADC conversions from the following sources: firmware, DPWM rising edge, ADC_EXT_TRIG pin or Analog Comparator results
- Interrupt capability to embedded processor at completion of ADC conversion
- Six digital comparators on the first 6 channels of the conversion sequence using either raw ADC data or averaged ADC data
- Two 10 µA current sources for excitation of PMBus addressing resistors
- Dual sample and hold for accurate power measurement
- Internal temperature sensor for temperature protection and monitoring

The control module *ADC12 Contol Block Diagram* contains the control and conversion logic for auto-sequencing a series of conversions. The sequencing is fully configurable for any combination of 16 possible ADC channels through an analog multiplexer embedded in the ADC12 block. Once converted, the selected channel value is stored in the result register associated with the sequence number. Input channels can be sampled in any desired order or programmed to repeat conversions on the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in order of conversion, where the result 0 register is the first conversion of a 16-channel sequence and result 15 register is the last conversion of a 16-channel sequence. The number of channels converted in a sequence can vary from 1 to 16.

Unlike EADC0 through EADC2, which are primarily designed for closing high speed compensation loops, the ADC12 is not usually used for loop compensation purposes. The EADC converters have a substantially faster conversion rate, thus making them more attractive for closed loop control. The ADC12 features make it best suited for monitoring and detection of currents, voltages, temperatures and faults. Please see the *Typical Characteristics* plots for the temperature variation associated with this function.

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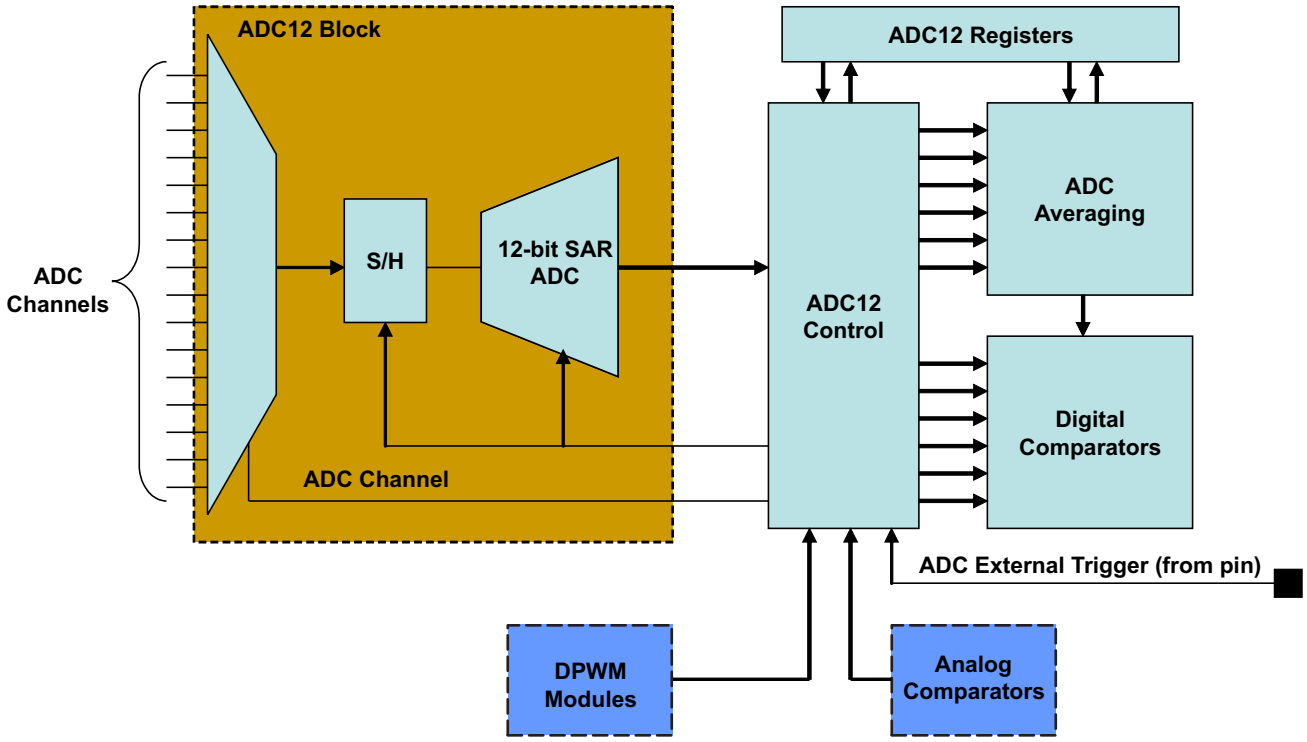

Figure 6-19. ADC12 Control Block Diagram

6.10.4 Timers

External to the Digital Power Peripherals there are 3 different types of timers in UCD3138A. They are the 24-bit timer, 16-bit timer and the Watchdog timer

6.10.4.1 24-bit PWM Timer

There is one 24 bit counter PWM timer which runs off the Interface Clock and can further be divided down by an 8-bit pre-scalar to generate a slower PWM time period. The timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, the timer has a shadow register (Data Buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The two capture pins TCMP0 and TCMP1 are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin. Upon this event, the counter value is stored in the corresponding capture data register.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by software controlled register. Five Interrupts from the PWM timer can be set, which are the counter rollover event (overflow), either capture event 0 or 1, or the two comparison match events. Each interrupt can be disabled or enabled.

Upon an event comparison on only the second event, the TCMP pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as general purpose I/O for reading the value of the input at the pin. The first compare event can only be used as an interrupt.

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6.10.4.2 16-Bit PWM Timers

There are four 16 bit counter PWM timers which run off the Interface Clock and can further be divided down by a 8-bit pre-scaler to generate slower PWM time periods. Each timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, each timer has a shadow register (Data Buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The counter reset can be configured to happen on a counter roll over, a compare equal event, or by a software controlled register. Interrupts from the PWM timer can be set due to the counter rollover event (overflow) or by the two comparison match events. Each comparison match and the overflow interrupts can be disabled or enabled.

Upon an event comparison, the PWM pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as General Purpose I/O for reading the value of the input at the pin.

6.10.4.3 Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked off of a separate low speed oscillator source. If the timer is allowed to expire, a reset condition is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power-up the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half timer flag is also provided for status monitoring of the watchdog.

6.11 Miscellaneous Analog

The Miscellaneous Analog Control (MAC) Registers provide control and monitor a wide variety of functions. These functions include device supervisory features such as Brown-Out and power saving configuration, general purpose input/output configuration and interfacing, internal temperature sensor control and current sharing control.

The MAC module also provides trim signals to the oscillator and AFE blocks. These controls are usually used at the time of trimming at manufacturing; therefore this document will not cover these trim controls.

The MAC registers and peripherals are all available in the UCD3138A (64 pin version). Other UCD3138A devices may have reduced resources. See the device pin out description for details.

6.12 Package ID Information

Package ID register includes information regarding the package type of the device and can be read by firmware for reporting through PMBus or for other package sensitive decisions.

BIT NUMBER	1:0
Bit Name	PKG_ID
Access	R/W
Default	0 – UCD3138ARGC, 1 – UCD3138ARHA

6.13 Brownout

Brownout function is used to determine if the device supply voltage is lower than a threshold voltage, a condition that may be considered unsafe for proper operation of the device.

The brownout threshold is higher than the reset threshold voltage; therefore, when the supply voltage is lower than brownout threshold, it still does not necessarily trigger a device reset.

The brownout interrupt flag can be polled or alternatively can trigger an interrupt to service such case by an interrupt service routine. See *Section 5.7*.

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6.14 Global I/O

Up to 30 pins in UCD3138A can be configured to serve as a general purpose input or output pin (GPIO). This includes all digital input or output pins except for the RESET pin.

The pins that cannot be configured as GPIO pins are the supply pins, ground pins, ADC-12 analog input pins, EADC analog input pins and the RESET pin.

There are two ways to configure and use the digital pins as GPIO pins:

1. Through the centralized Global I/O control registers.
2. Through the distributed control registers in the specific peripheral that shares it pins with the standard GPIO functionality.

The Global I/O registers offer full control of:

1. Configuring each pin as a GPIO.
2. Setting each pin as input or output.
3. Reading the pin's logic state, if it is configured as an input pin.
4. Setting the logic state of the pin, if it is configured as an output pin.
5. Configuring pin/pins as open drain or push-pull (Normal)

The Global I/O registers include Global I/O EN register, Global I/O OE Register, Global I/O Open Drain Control Register, Global I/O Value Register and Global I/O Read Register.

The following is showing the format of Global I/O EN Register (GLBIOEN) as an example:

BIT NUMBER	29:0
Bit Name	GLOBAL_IO_EN
Access	R/W
Default	00_0000_0000_0000_0000_0000_0000_0000

Bits 29-0: GLOBAL_IO_EN – This register enables the global control of digital I/O pins
0 = Control of IO is done by the functional block assigned to the IO (Default)
1 = Control of IO is done by Global IO registers.

BIT	PIN_NAME	PIN NUMBER	
		UCD3138A-64 PINS	UCD3138A-40 PINS
29	FAULT[3]	43	NA
28	ADC_EXT_TRIG	12, 26	8
27	TCK	37	21
26	TDO	38	20
25	TMS	40	24
24	TDI	39	23
23	SCI_TX[1]	29	NA
22	SCI_TX[0]	14	22
21	SCI_RX[1]	30	NA
20	SCI_RX[0]	13	23
19	TMR_CAP	12, 26, 41	8, 21
18	TMR_PWM[1]	32	NA
17	TMR_PWM[0]	12, 26, 31, 37	21
16	PMBUS-CLK	15	9
15	PMBUS-DATA	16	10
14	CONTROL	30	20
13	ALERT	29	19
12	EXT_INT	26, 34	NA

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BIT	PIN_NAME	PIN NUMBER	
		UCD3138A-64 PINS	UCD3138A-40 PINS
11	FAULT[2]	42	25
10	FAULT[1]	36	23
9	FAULT[0]	35, 39	22
8	SYNC	12, 26,37	8, 21
7	DPWM3B	24	18
6	DPWM3A	23	17
5	DPWM2B	22	16
4	DPWM2A	21	15
3	DPWM1B	20	14
2	DPWM1A	19	13
1	DPWM0B	18	12
0	DPWM0A	17	11

6.15 Temperature Sensor Control

Temperature sensor control register provides internal temperature sensor enabling and trimming capabilities. The internal temperature sensor is disabled as default.

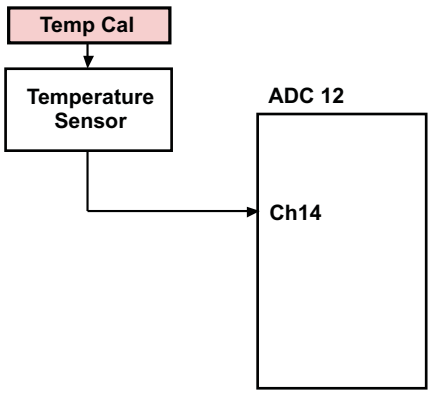

Figure 6-20. Internal Temp Sensor

Temperature sensor is calibrated at room temperature (25°C) via a calibration register value.

The temperature sensor is measured using ADC12 (via Ch14). The temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds a delta to the ADC measurement).

The temperature sensor can be enabled or disabled.

6.16 I/O Mux Control

In different packages of UCD3138A several I/O functions are multiplexed and routed toward a single physical pin. I/O Mux Control register may be used in order to choose a single specific functionality that is desired to be assigned to a physical device pin for your application.

6.17 Current Sharing Control

UCD3138A provides three separate modes of current sharing operation.

- Analog bus current sharing
- PWM bus current sharing
- Master/Slave current sharing

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- AD02 has a special ESD protection mechanism that prevents the pin from pulling down the current-share bus if power is missing from the UCD3138A

The simplified current sharing circuitry is shown in the drawing below:

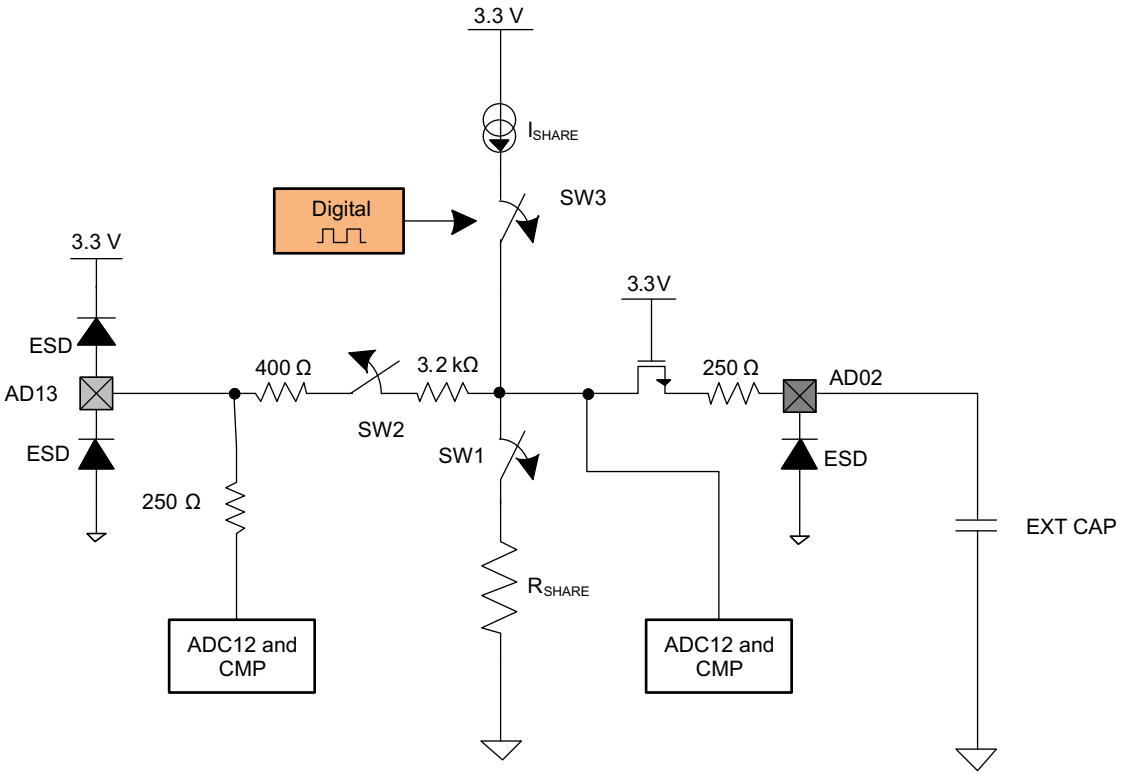

Figure 6-21. Simplified Current Sharing Circuitry

CURRENT SHARING MODE	FOR TEST ONLY, ALWAYS KEEP 00	CS_MODE	EN_SW1	EN_SW2	DPWM
Off or Slave Mode (3-state)	00	00 (default)	0	0	0
PWM Bus	00	01	1	0	ACTIVE
Off or Slave Mode (3-state)	00	10	0	0	0
Analog Bus or Master	00	11	0	1	0

The period and the duty of 8-bit PWM current source and the state of the SW1 and SW2 switches can be controlled through the current sharing control register (CSCTRL).

6.18 Temperature Reference

The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 14) during the factory trim and calibration.

This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost.

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7 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The UCD3138A has an extensive set of fully-programmable, high-performance peripherals that make it suitable for a wide range of power supply applications. In order to make the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device for several key applications. In each case the following items are available:

1. Full featured EVM hardware that demonstrates classic power supply functionality.
2. An EVM user guide that contains schematics, bill-of-materials, layout guidance and test data showcasing the performance and features of the device and the hardware.
3. A firmware programmers manual that provides a step-by-step walk through of the code.

Table 7-1. Application Information

APPLICATION	EVM DESCRIPTION
Phase shifted full bridge	This EVM demonstrates a PSFB DC-DC power converter with digital control using the UCD3138A device. Control is implemented by using PCMC with slope compensation. This simplifies the hardware design by eliminating the need for a series blocking capacitors and providing the inherent input voltage feed-forward that comes from PCMC. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 360 W, or full output current of 30 A.
LLC resonant converter	This EVM demonstrates an LLC resonant half-bridge DC-DC power converter with digital control using the UCD3138A device. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 340 W, or full output current of 29 A.

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7.2 Typical Application

This section summarizes the PSFB EVM DC-DC power converter.

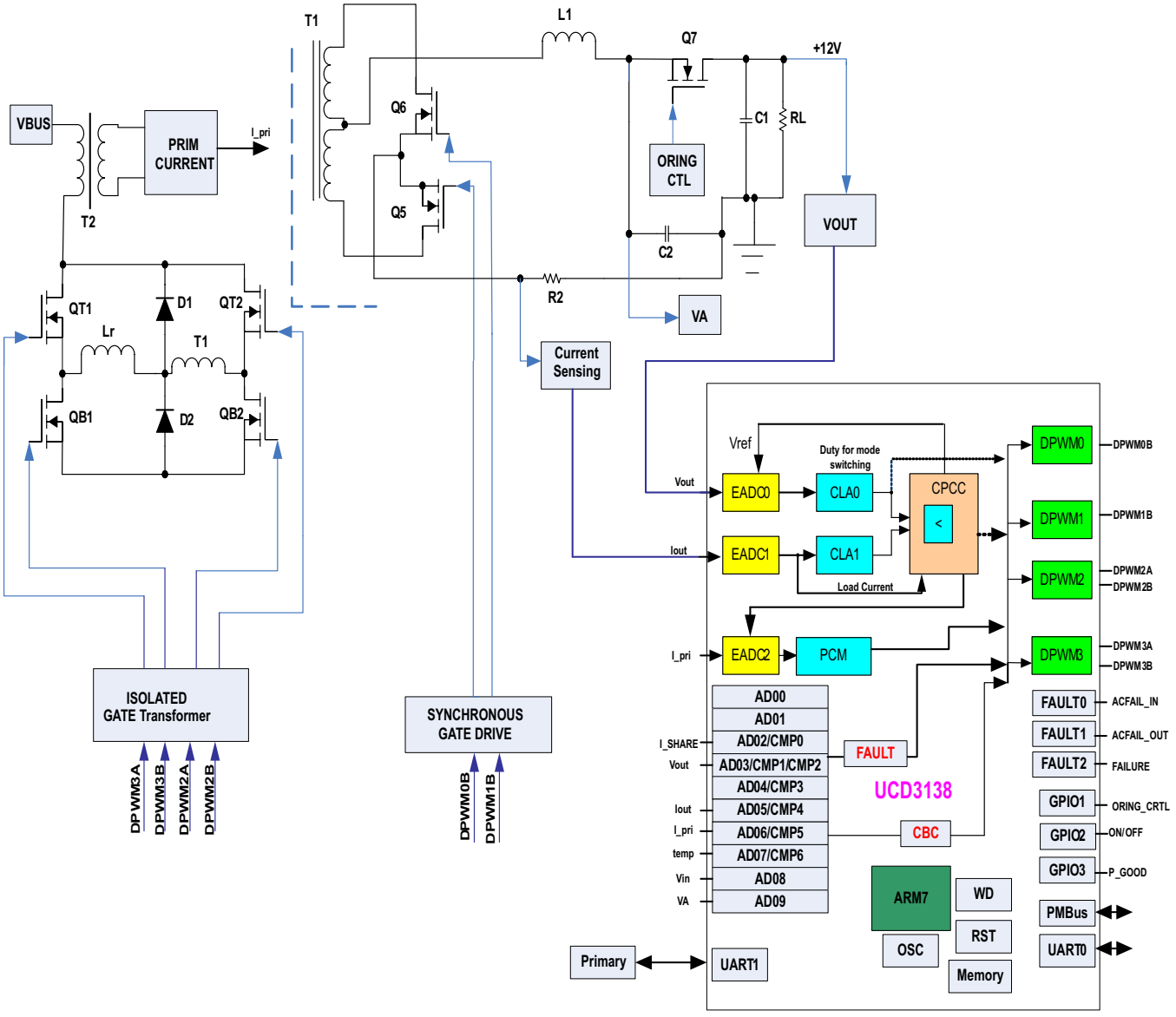

Figure 7-1. Phase-Shifted Full-Bridge

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7.2.1 Design Requirements

Table 7-2. Input Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_{in}	Input voltage range	Normal Operating	350	385	420	V
V_{inmax}	Max input voltage	Continuous			420	V
I_{in}	Input current	Vin=350V, Full Load		1.15		A
I_{stby}	Input no load current	Output current is 0A		30		mA
V_{on}	Undervoltage lockout	V_{in} Decreasing (input voltage is detected on secondary side)		340		V
V_{hys}		V_{in} Increasing		360		V

Table 7-3. Output Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_O	Output voltage setpoint	No load on outputs		12		V
Reg_{line}	Line regulation	All outputs; 360 ≤ V_{in} ≤ 420; I_O = I_{Omax}			0.5%	
Reg_{load}	Load regulation	All outputs; 0 ≤ I_O ≤ I_{Omax}; V_{in} = 400 V			1%	
V_n	Ripple and noise(1)	5 Hz to 20 MHz		100		mVpp
I_O	Output current		0		30	A
η	Efficiency at phase-shift mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at PWM ZVS mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at hard switching mode	Vo = 12 V, Io = 15 A		90%		
V_{adj}	Output adjust range		11.4		12.6	V
V_{tr}	Transient response overshoot/undershoot	50% load step at 1 AμS, min load at 2 A		±0.36		V
$t_{settling}$	Transient response settling time			100		μS
t_{start}	Output rise time	10% to 90% of Vout		50		mS
	Overshoot	At startup			2%	
fs	Switching frequency	Over V_{in} and I_O ranges		150		kHz
I_{share}	Current sharing accuracy	50% - Full load		±5%		
φ	Loop phase margin	10% - Full load		45		°
G	Loop gain margin	10% - Full load		10		dB

(1) Ripple and noise are measured with 10-μF Tantalum capacitor and 0.1-μF ceramic capacitor across output.

7.2.2 Detailed Design Procedure

7.2.2.1 PCMC (Peak Current Mode Control) PSFB (Phase-Shifted Full Bridge) Hardware Configuration Overview

The hardware configuration of the UCD3138A PCMC PSFB converter contains two critical elements that are highlighted in the subsequent sections.

- DPWM initialization - This section will highlight the key register settings and considerations necessary for the UCD3138A to generate the correct MOSFET waveforms for this topology. This maintains the proper phase relationship between the MOSFETs and synchronous rectifiers as well as the proper set up required to function correctly with PCMC.
- PCMC initialization - This section will discuss the register settings and hardware considerations necessary to modulate the DPWM pins with PCMC and internal slope compensation.

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7.2.2.2 DPWM Initialization for PSFB

The UCD3138A DPWM peripheral provides flexibility for a wide range of topologies. The PSFB configuration utilizes the Intra-Mux and Edge Generation Modules of the DPWM. For a diagram showing these modules, see the UCD3138A Digital Power Peripherals Manual.

Here is a schematic of the power stage of the PSFB:

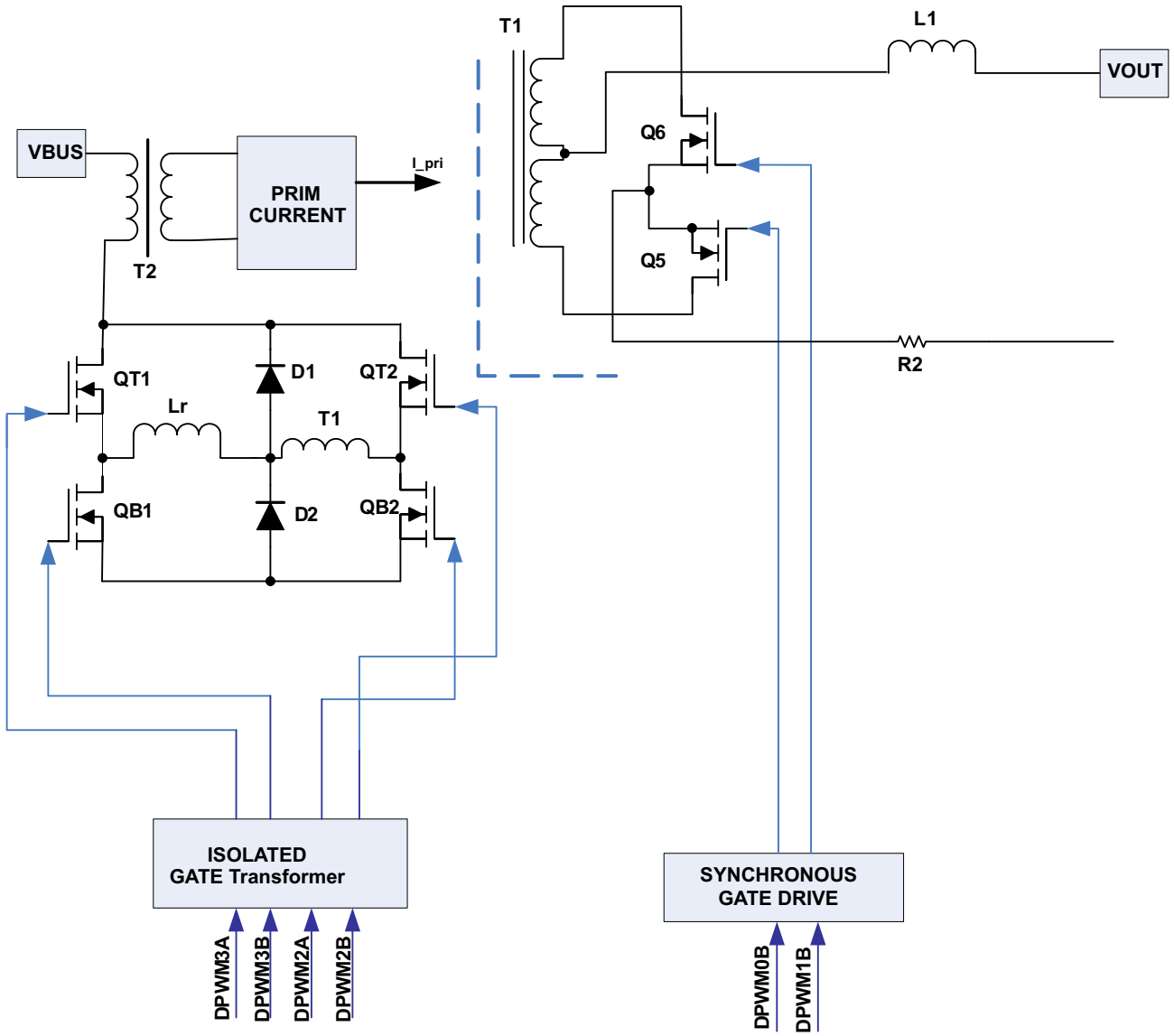

Figure 7-2. Schematic – PSFB Power Stage

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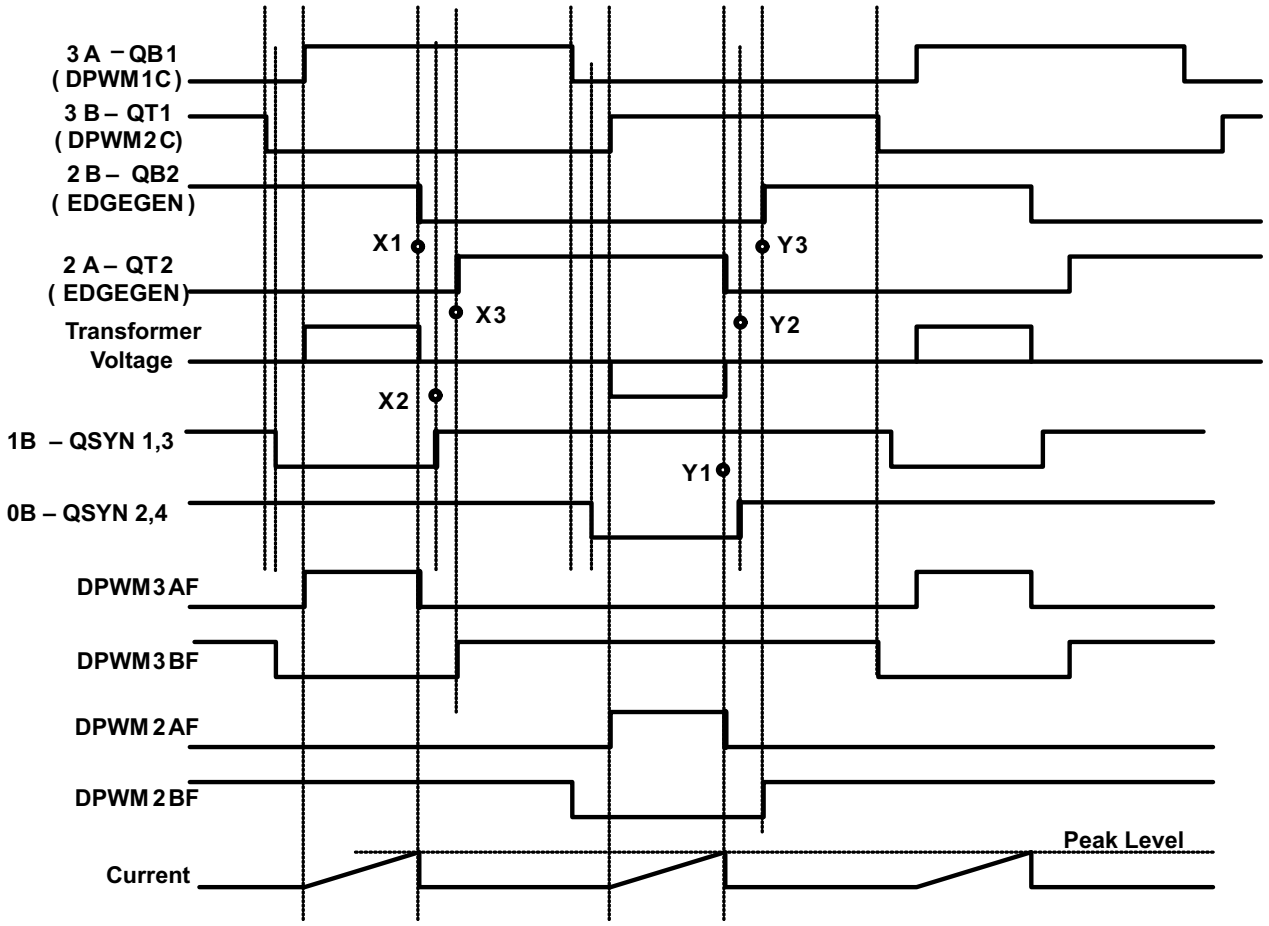
Here is an overview of the key PSFB signals:



X 1 , X 2 , X 3 and Y 1 , Y 2 , Y 3 are sets of moving edges. All other edges are fixed

Figure 7-3. Key PSFB Signals

7.2.3 DPWM Synchronization

DPWM1 is synchronized to DPWM0, DPWM2 is synchronized to DPWM1, and DPWM3 is synchronized to DPWM2, ½ period out of phase using these commands:

```
Dpwm1Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; //configured to slave
Dpwm2Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave
Dpwm3Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave

Dpwm0Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm1Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm2Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;

LoopMuxRegs.DPWMMUX.bit.DPWM1_SYNC_SEL    // Slave to dpwm-0
= 0;                                      // Slave to dpwm-1
LoopMuxRegs.DPWMMUX.bit.DPWM2_SYNC_SEL    // Slave to dpwm-2
= 1;
LoopMuxRegs.DPWMMUX.bit.DPWM3_SYNC_SEL
= 2;
```

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If the event registers on the DPWMs are the same, the two pairs of signals will be symmetrical. All code examples are taken from the PSFB EVM code, unless otherwise stated.

7.2.4 Fixed Signals to Bridge

The two top signals in the above drawing have fixed timing. The DPWM1CF and DPWM2CF signals are used for these pins. DPWMCxF refers to the signal coming out of the fault module of DPWMx, as shown in Figure 7-4.

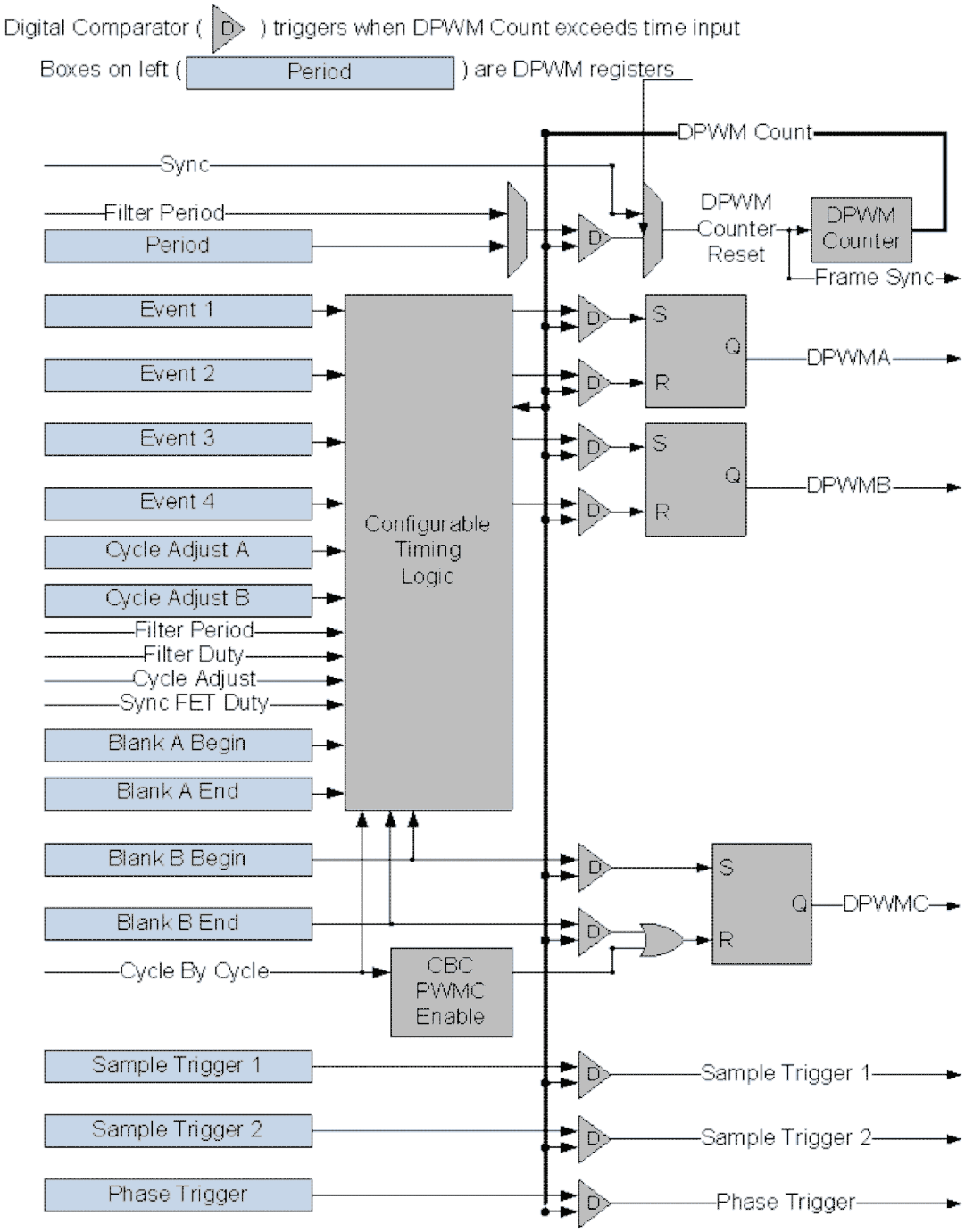

Figure 7-4. Fixed Signals to Bridge

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These signals are actually routed to pins DPWM3A and 3B using the Intra Mux with these statements:

```
Dpwm3Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 7; // Send DPWM1C
Dpwm3Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 8; // Send DPWM2C
```

Since these signals are really being used as events in the timer, the #defines are called EV5 and EV6. Here are the statements which initialize them:

```
// Setup waveform for DPWM-C (re-using blanking B regs)
Dpwm2Regs.DPWMBLKBBEG.all = PWM2_EV5 + (4 *16);
Dpwm2Regs.DPWMBLKBEND.all = PWM2_EV6;
```

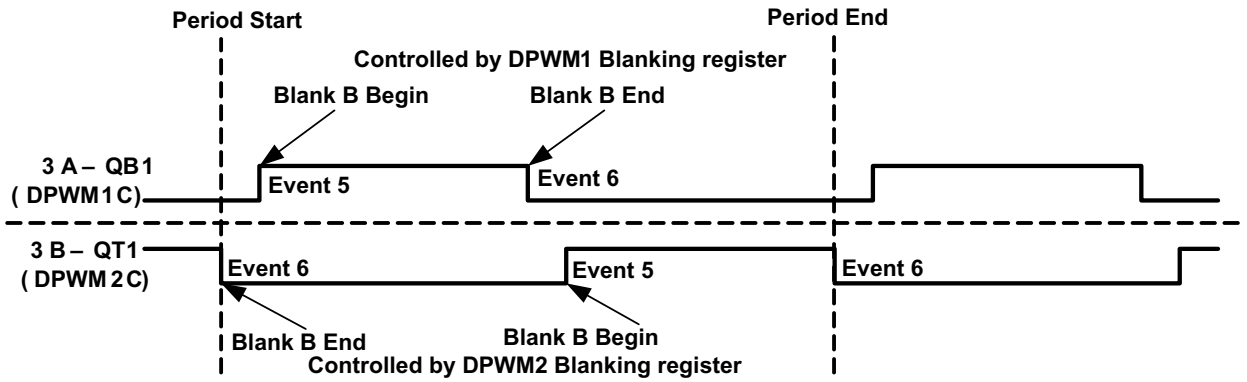


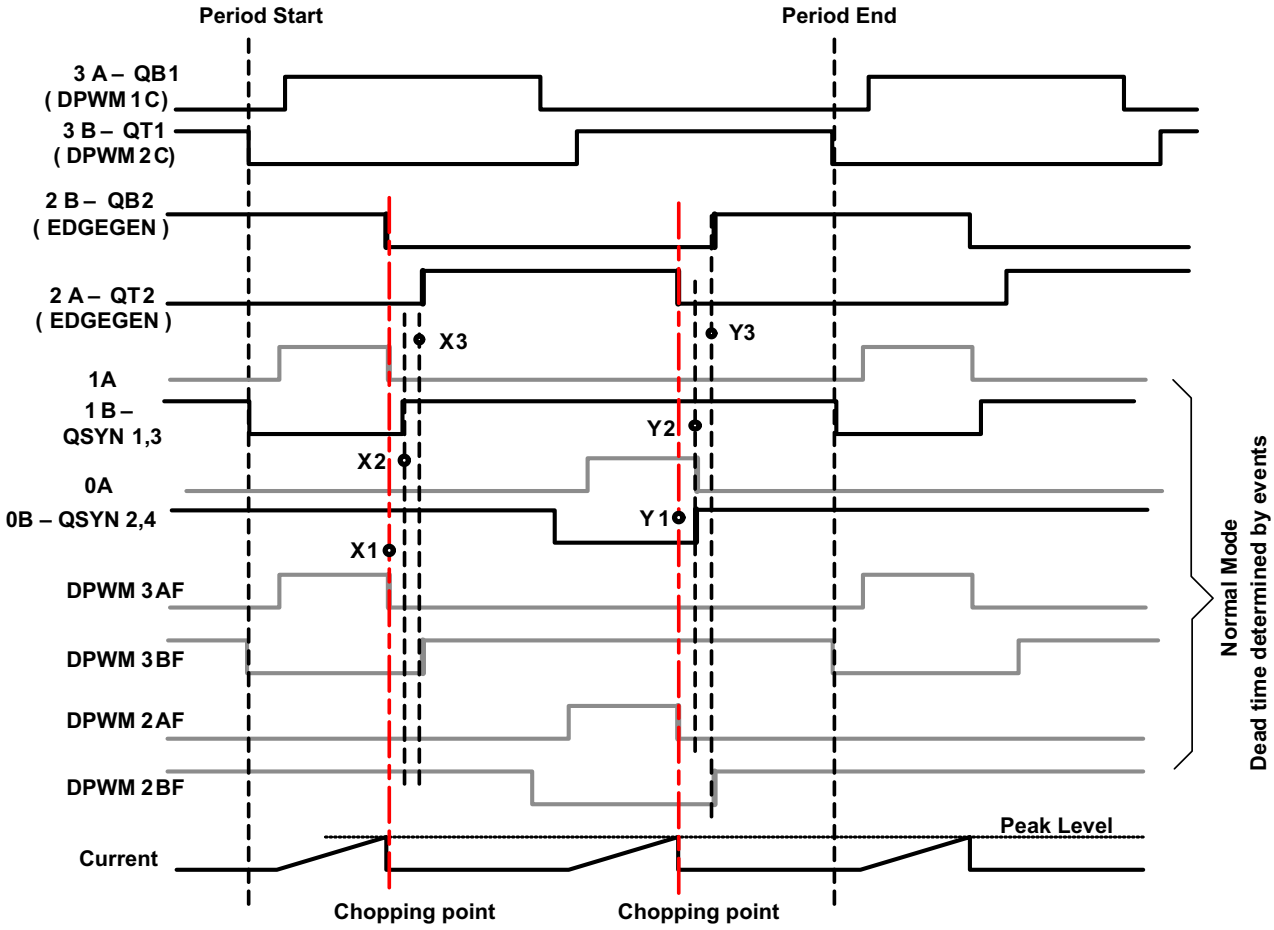
Figure 7-5. Blank B Timing Information

The statements for DPWM1 are the same. Remember that DPWMC reuses the Blank B registers for timing information.

7.2.5 Dynamic Signals to Bridge

DPWM0 and 1 are set at normal mode. PCMC triggering signal (fault) chops DPWM0A and 1A cycle by cycle. The corresponding DPWM0B and 1B are used for synchronous rectifier MOSFET control. The same PCMC triggering signal is applied to DPWM2 and DPWM3. Both of these are set to normal mode as well. DPWM2 and 3 are chopped and their edges are used to generate the next two dynamic signals to the bridge. They are generated using the Edge Generator Module in DPWM2. The Edge Generator sources are DPWM2 and DPWM3. The edges used are:

DPWM2A turned on by a rising edge on DPWM2BF
DPWM2A turned off by a falling edge on DPWM3AF
DPWM2B turned on by a rising edge on DPWM3BF
DPWM2B turned off by a falling edge on DPWM2AF



X 1 , X 2 , X 3 and Y 1 , Y 2 , Y 3 are sets of moving edges. All other edges are fixed

Figure 7-6. Dynamic Signals to Bridge

The Edge Generator is configured with these statements:

```
Dpwm2Regs.DPWMEDGEGEN.bit.A_ON_EDGE = 2;
Dpwm2Regs.DPWMEDGEGEN.bit.A_OFF_EDGE = 5;
Dpwm2Regs.DPWMEDGEGEN.bit.B_ON_EDGE = 6;
Dpwm2Regs.DPWMEDGEGEN.bit.B_OFF_EDGE = 1;

Dpwm2Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 1; // EDGEGEN-A out the A output
Dpwm2Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 1; // EDGEGEN-B out the B output

Dpwm2Regs.DPWMEDGEGEN.bit.EDGE_EN = 1;
```

The EDGE_EN bits are set for all 4 DPWMs. This is done to ensure that all signals have the same timing delay through the DPWM.

The finial 6 gate signals are shown in Figure 7-7.

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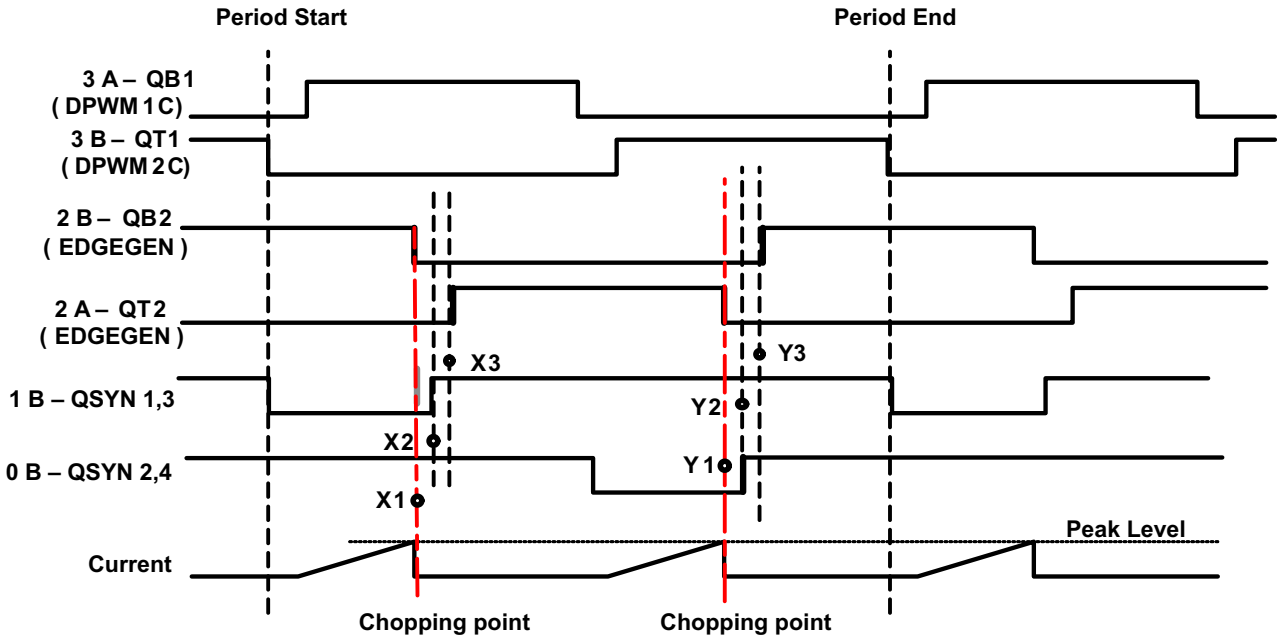

Figure 7-7. Final 6 Gate Signals

Note how the falling edge of DPWM2AF aligns with the X1 edge, and how the rising edge of DPWM2BF aligns with the X3 edge. The falling edges on DPWM2AF and DPWM3AF are caused by the peak detection logic. This is fed through the Cycle By Cycle logic. The Cycle By Cycle logic also has a special feature to control the rising edges of DPWM2BF (X1 and X3) and DPWM3BF (Y1 and Y3). It uses the value of Event3 – Event2 to control the time between the edges. The same feature is used with DPWM0 and DPWM1 to control the X2 and Y2 signals. Using the other 2 DPWMs permits these signals to have a different dead time.

The same setup can be used for voltage mode control. In this case, the Filter output sets the timing of the falling edge on DPWMxAF.

All DPWMs are configured in Normal mode, with CBC enabled. If external slope compensation is used, DPWM1A and DPWM1B are used to reset the external compensator at the beginning of each half cycle. If no PCMC event occurs, the values of Events 2 and 3 determine the locations of the edges, just as in open loop mode.

7.2.6 System Initialization for PCM

PCM (Peak Current Mode) is a specialized configuration for the UCD3138A which involves several peripherals. This section describes how it works across the peripherals.

7.2.6.1 Use of Front Ends and Filters in PSFB

All three front ends are used in PSFB. The same signals are used in the same places for both PCMC and voltage mode. The same hardware can be used for both control modes, with the mode determined by which firmware is loaded into the device. FE0 and FE1 are used with their associated filters, but Filter 2 is not used at all.

FE0 – Vout – voltage loop
FE1 – Iout – current loop
FE2 – Ipri – PCM

In PCMC mode, FE2 is used for PCMC, and the voltage loop is normally used to provide the start point for the compensation ramp. If the CPCC firmware detects a need for constant current mode, it switches to the current loop for the start point.

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7.2.6.2 Peak Current Detection

Peak current detection involves all the major modules of the DPPs, the Front End, Filter, Loop Mux, Fault Mux and the DPWMs. A drawing of the major elements is shown in Figure 7-8.

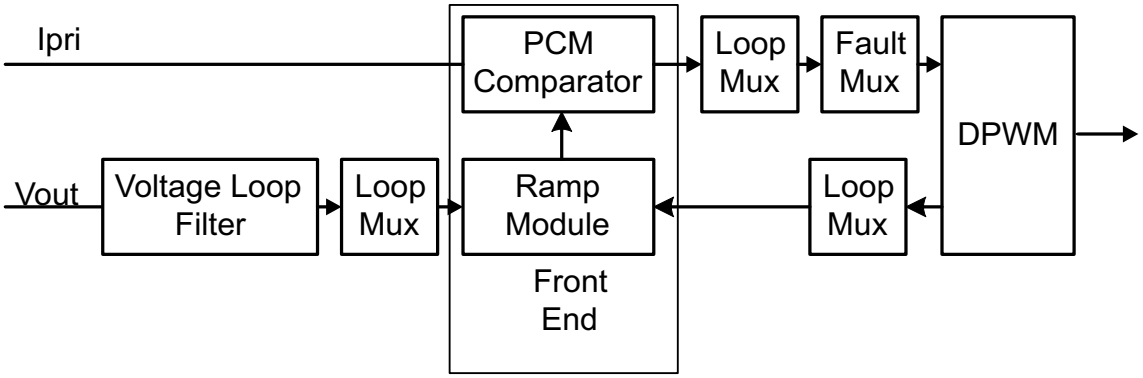

Figure 7-8. Peak Current Detection Function

The voltage loop is used to select a peak current level. This level is fed to the Ramp module to generate a compensation ramp. The compensation ramp is compared to the primary current by the PCMC comparator in the Front End. When the ramp value is greater than the primary current, the APCMC signal is sent to the DPWM, causing the events described in the previous sections.

The DPWM frame start and output pin signals can be used to trigger the Ramp Module. In this case, each DPWM frame triggers the start of the ramp. The ramp steps every 32 ns.

The PCM_FILTER_SEL bits in the LoopMux.PCMCTRL register are used to select which filter is connected to the ramp module:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =0; //select filter0
```

With Firmware Constant Power/Constant current, Filter 1 and Front End 1 are used as a current control loop, with the EADCDAC set to high current. If the voltage loop value becomes higher than the current loop value, then Filter 1 is used to control the PCM ramp start value:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =1;
        //select filter1 for slope compensation source
```

In the ramp module, there are 2 bitfields in the RAMPCTRL register which must be configured. The PCM_START_SEL must be set to a 1 to enable the Filter to be used as a ramp start source. The RAMP_EN bit must be set, of course.

The DAC_STEP register sets the slope of the compensation ramp. The DAC value is in volts, of course, so it is necessary to calculate the slope after the current to voltage conversion. Here is the formula for converting from millivolts per microsecond to DACSTEP.

m = compensation slope in millivolts per microsecond

$ACSTEP = 335.5 \times M$

In C, this can be written:

```
#define COMPENSATION_SLOPE 150 //compensation slope in millivolts per microsecond
#define DACSTEP_COMP_VALUE ((int) (COMPENSATION_SLOPE*335.5) )
        //value in DACSTEP for desired compensation slope

        FeCtrl0Regs.DACSTEP.all = DACSTEP_COMP_VALUE;
```

It may also be necessary to set a ramp ending value in the RAMPDACEND register.

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In addition, it is necessary to set the D2S_COMP_EN bit in the EADCCTRL register. This is for enabling the differential to single ended comparator function. The front end diagram leaves it out for simplicity, but the connection between the DAC and the EADC amplifier is actually differential. The PCMC comparator, however, is single ended. So a conversion is necessary as shown in Figure 7-9.

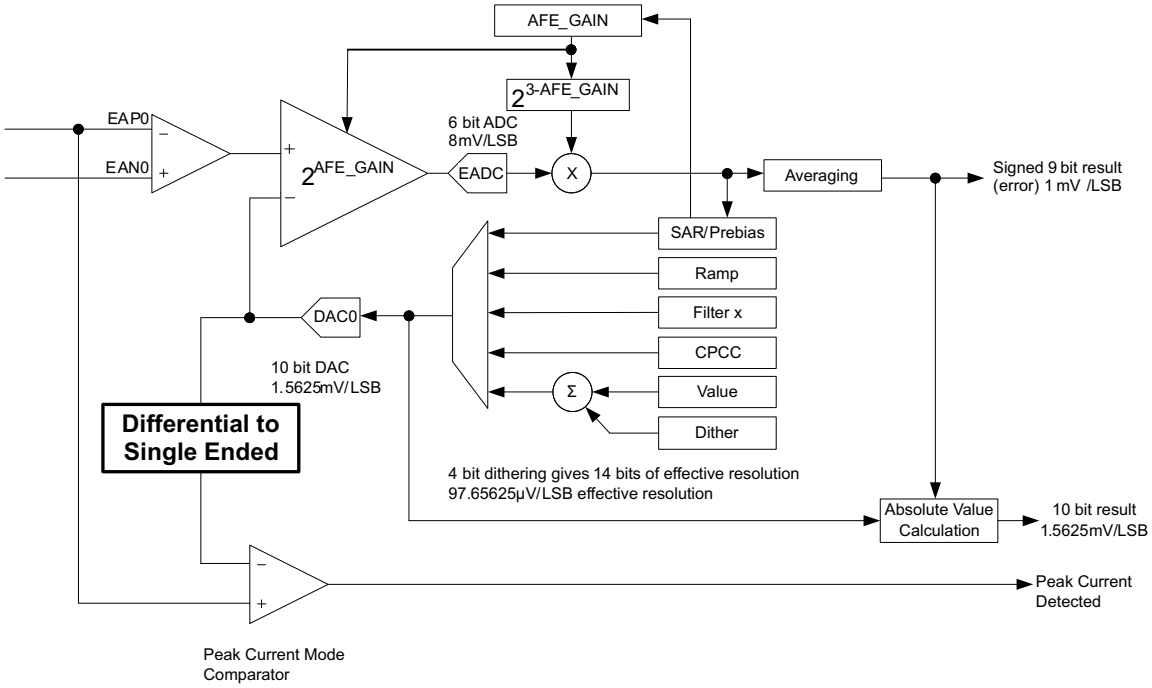


Figure 7-9. Differential to Single-Ended Comparator Function

The EADC_MODE bit in EADCCTRL should be set to a 5 for peak current mode.

The peak current detection signal next goes to the Loop Mux. The Fault Mux has only 1 APCM input, but there are 3 front ends. So the PCM_FE_SEL bits in APCMCTRL must be used to select which front end is used:

LoopMuxRegs.APCMCTRL.bit.PCM_FE_SEL = 2; // use FE2 for PCM */

The PCM_EN bit must also be set.

LoopMuxRegs.APCMCTRL.bit.PCM_EN = 1; // Enable PCM

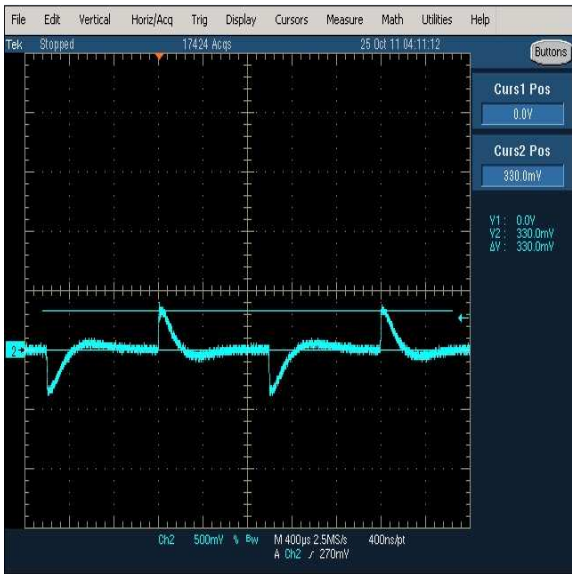
Next the Fault Mux is used to enable the APCM bit to the CLIM/CBC signal to the DPWM. There are 4 DPWMxCLIM registers, one for each DPWM. The ANALOG_PCM_EN bit must be set in each one to connect the PCM detection signal to the CLIM/CBC signal on each DPWM. For the latest configuration information on all of these bits, consult the appropriate EVM firmware. To avoid errors, it is best to configure your hardware design using the same DPWMs, filters, and front ends for the same functions as the EVM.

DPWM timing is used to trigger the start of the ramp. This is selected by the FECTRLxMUX registers in the Loop Mux. DPWMx_FRAME_SYNC_EN bits, when set, cause the ramp to be triggered at the start of the DPWM period.

7.2.6.3 Peak Current Mode (PCM)

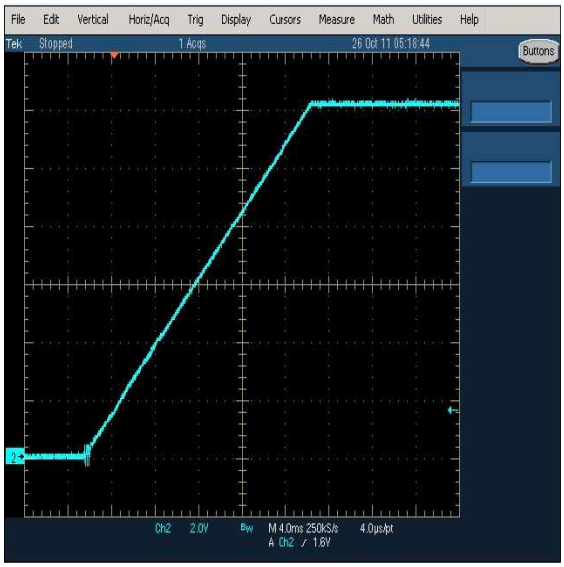
There is one peak current mode control module in the device however any front end can be configured to use this module.

7.2.7 Application Performance Plots



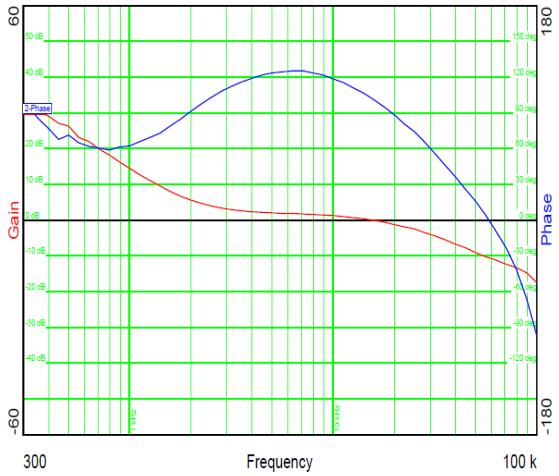
1A-16A-1A Vin =385V

Figure 7-10. Load Transient



30A Load syncFETs off

Figure 7-11. V_{OUT} Soft Start



Kp =14000
Ki =300

Kd =2000

Alpha = –2

Figure 7-12. Bode Plot

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7.3 Layout

7.3.1 Layout Guidelines

- Single ground is recommended: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path, referred to the layout example.
- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, Capacitance and ESR, and they have different frequency response.
- Avoid long traces close to radiation components, and place them into an internal layer, and it is preferred to have grounding shield, and in the end, add a termination circuit;
- Analog circuit such as ADC sensing lines needs a return current path into the analog circuitry; digital circuit such as GPIO, PMBus and PWM has a return current path into the digital circuitry; although with a single plane, still try to avoid to mix analog current and digital current.
- Don't use a ferrite bead or larger than 3 Ω resistor to connect between V33A and V33D.
- Both 3.3VD and 3.3VA should have local 4.7 µF decoupling capacitors close to the device power pins, add visas to connect decoupling caps directly to SGND.
- Avoid negative current/negative voltage on all pins, so Schottky diodes may need to clamp the voltage; avoid the voltage spike on all pins more than 3.8 V or less than –0.3 V, add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that a Schottky has relatively higher leakage current, which can affect the voltage sensing at high temperature.
- $\overline{\text{RESET}}$ pin should have one at least 2.2 µF low ESL capacitor locally decoupled with SGND plane. This capacitor must be located close to the device $\overline{\text{RESET}}$ pin. It is highly recommended to use a small resistance (such as 220 Ω) to connect the $\overline{\text{RESET}}$ pin with 3.3 VD.

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7.3.2 Layout Example

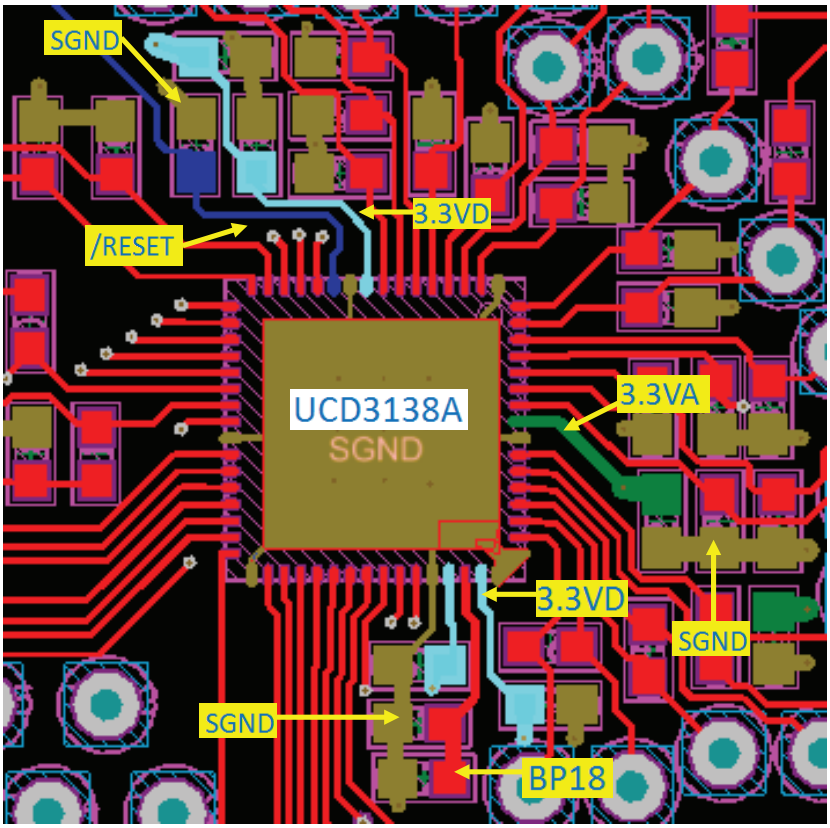

Figure 7-13. UCD3138A Layout Example

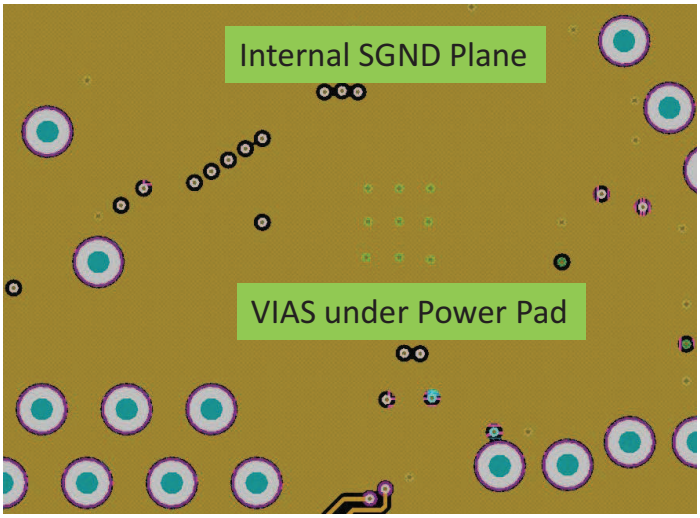

Figure 7-14. UCD3138A Layout Example, Internal Plane

7.4 Power Supply Decoupling and Bulk Capacitors

- Both 3.3 VD and 3.3 VA should have a local 4.7-µF capacitor placed as close as possible to the device pins.
- BP18 should have a 1-µF capacitor.

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8 器件和文档支持

8.1 器件支持

8.1.1 开发支持

TI 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。 工具的电子支持文档可从 Code Composer Studio™ 集成开发环境 (IDE) 中获得。

以下产品支持开发*您的器件*器件应用：

软件开发工具：Code Composer Studio™ 集成开发环境 (IDE)：其中包括支持任意*您的器件*器件应用所需的编辑器、C/C++/汇编代码生成工具、调试工具以及能够提供基本运行时目标软件的可扩展实时基础软件 (DSP/BIOS™)。

硬件开发工具：扩展开发系统 (XDS™) 仿真器

有关*您的器件*平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com。 有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。

8.1.1.1 工具和文档

UCD3138A 应用固件在德州仪器 (TI) Code Composer Studio (CCS) 集成开发环境（建议采用版本 v6.x）中开发。

特定电源拓扑的器件编程、实时调试以及主要器件参数的监视/配置工作都可通过德州仪器 (TI) 的 FUSION_DIGITAL_POWER_DESIGNER 图形用户界面进行 (http://www.ti.com/tool/fusion_digital_power_designer)。

FUSION_DIGITAL_POWER_DESIGNER 软件应用采用 PMBus 协议通过串行总线与器件通信，所使用的接口适配器为德州仪器 (TI) 评估模块 (EVM) USB-TO-GPIO (http://www.ti.com/tool/usb-to-gpio)。FUSION_DIGITAL_POWER_DESIGNER GUI 的器件 GUI 模块中的“内存调试器”工具可提供基于 PMBUS 的实时调试功能，这是替代基于 JTAG 的传统方法的有效选择。

该软件应用还可用于器件编程，所使用的工具是针对生产环境进行优化的 FUSION_MFR_GUI (http://www.ti.com/tool/fusion_mfr_gui)。 FUSION_MFR_GUI 工具支持多个板载器件，且具有内置记录和报告功能。

在参考文档方面，以下 3 本编程手册可提供关于 UCD3138A 数字控制器应用和使用方法的详细信息：

1. 本手册中涵盖的 UCD3138A 数字电源外设编程手册关键主题包括：
   - 数字脉宽调制器 (DPWM)
     - 工作模式（正常/多相/相移/谐振等）
     - 自动模式切换
     - 数字脉宽调制控制器 (DPWMC)、边沿生成和内部多路复用
   - 前端
     - 模拟前端
     - ADC 或 EADC 误差
     - 前端 DAC
     - 斜坡模块
     - 逐次逼近寄存器模块
   - 滤波器
     - 滤波器数学函数
   - 环路复用
     - 模拟峰值电流模式
     - 恒定电流/恒定功率 (CCCP)
     - 自动周期调整
   - 故障复用
     - 模拟比较器
     - 数字比较器

  - 故障引脚功能
  - DPWM 故障动作
  - 理想二极管仿真 (IDE)，断续传导模式 (DCM) 检测
  - 振荡器故障检测
- UCD3138A 中上述全部外设的寄存器映射

2. 《UCD3138A 监视和通信编程手册》
   本手册中介绍的关键主题包括：
   - ADC12
     - 控制、转换、定序和取平均值
     - 数字比较器
     - 温度传感器
     - PMBUS 寻址
     - 双路采样和保持
   - 其它模拟控制（电流分流、欠压、时钟门控）
   - PMBUS 接口
   - 通用输入输出 (GPIO)
   - 定时器模块
   - PMBus
   - UCD3138A 中上述全部外设的寄存器映射
3. 《UCD3138A ARM 和数字系统编程手册》
   本手册中介绍的关键主题包括：
   - 引导 ROM 和引导闪存
     - BootROM 函数
     - 存储器读/写功能
     - 校验和函数
     - 闪存函数
     - 避免程序闪存锁定
   - ARM7 构架
     - 工作模式
     - 硬件/软件中断
     - 指令集
     - 两种内部工作状态（Thumb 16 位模式/ARM 32 位模式）
   - 存储器与系统模块
     - 地址解码器、DEC（存储器映射）
     - 存储器控制器 (MMC)
     - 中央中断模块
   - UCD3138A 中上述全部外设的寄存器映射
4. 《隔离电源应用 FUSION_DIGITAL_POWER_DESIGNER》
   - 设计者 GUI 用户指南
   - 器件 GUI 用户指南
   - 固件内存调试器
   - 生产工具 (MFR GUI)

除上述工具和文档外，如需获取有关评估模块、参考应用固件和应用手册/设计提示的最新信息，请访问 http://www.ti.com/product/UCD3138A。

8.1.1.2 开发套件

8.1.2 器件命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。 每个器件都具有以下三个前缀中的一个：X、P 或无（无前缀）（例如，*您的器件*）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。 这些前缀代表了产品开发的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

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器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发进化流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品.

TMDS 完全合格的开发支持产品。

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

为了指出产品开发周期的阶段，TI 为所有数字信号处理 (DSP) 器件和支持工具的部件号指定了前缀。 每一个 DSP 商用系列成员产品具有以下三个前缀中的一个：TMX、TMP、或者 TMS（例如，*您的器件*）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。 这些前缀代表了产品开发的发展阶段，即从工程原型（TMX 和 TMDX）直到完全合格的生产器件和工具（TMS 和 TMDS）。

器件开发进化流程：

TMX 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

TMP 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

TMS 完全合格的芯片模型的生产版本。

支持工具开发进化流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品.

TMDS 完全合格的开发支持产品。

TMX 和 TMP 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀表示封装类型（例如，*您的封装*），温度范围（例如，“空白”是默认的商业级温度范围）以及以 MHz 为单位的器件速度范围（例如，*您的器件的速度范围*）。图 8-1 提供了解读任一*您的器件*器件完整器件名称的图例。

要获得*您的封装*封装类型的*您的器件*器件订购部件号，请参见本文档的“封装选项附录”、（TI 网站 www.ti.com），或者联系您的 TI 销售代表。

有关芯片的器件命名标记的更多说明，请参见《*芯片勘误表*》（文献编号：SPRZxxx）。

图 8-1. 器件命名规则

8.2 文档支持

以下文档介绍*您的器件*处理器/MPU。 www.ti.com.cn 网站上提供了这些文档的副本。

SPRUxxx *技术参考手册*。 汇总了提供相关详细信息的文档。

SPRZxxx *芯片勘误表*。 说明了功能技术规格的已知例外情况。

8.2.1 参考文档

1. 《UCD3138A 数字电源外设编程手册》（文献编号：SLUU995）
2. 《UCD3138 监视和通信编程手册》（文献编号：SLUU996）

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3. 《UCD3138A ARM 和数字系统编程手册》（文献编号：SLUU994）
4. 《隔离电源应用 FUSION_DIGITAL_POWER_DESIGNER》（文献编号：SLUA676）
5. Code Composer Studio 开发工具 v3.3 – 入门指南（文献编号：SPRU509）
6. ARM7TDMI-S 技术参考手册
7. 系统管理总线 (SMBus) 技术规范
8. PMBus™ 电源系统管理协议规范

8.2.2 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

TI E2E™ 在线社区 ***TI 工程师对工程师 (E2E) 社区。*** 此社区的创建目的是为了促进工程师之间协作。 在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

德州仪器 (TI) 嵌入式处理器维基网站 ***德州仪器 (TI) 嵌入式处理器维基网站。*** 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.3 商标

Code Composer Studio, Fusion Digital Power, E2E are trademarks of Texas Instruments.
ARM7TDMI-S is a trademark of ARM.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

8.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械封装和可订购信息

9.1 Via Channel

[*您的封装*] 封装采用 Via Channel 技术进行了特别设计。 这使得 PCB 设计中能够采用 0.65mm 间距封装，实现比正常尺寸更大的 PCB 过孔和布线，从而减小 PCB 信号层数，并大幅降低 PCB 成本。 由于 Via Channel BGA 技术提升了分层效率，因此该器件允许仅在两个信号层（共四层）中进行 PCB 布线。

利用 [*所用封装*] 封装中实施的 Via Channel 技术可构建基于 [*所用器件*] 的产品，该产品采用 4 层 PCB 设计，但这可能达不到系统性能目标要求。 因此，产品设计期间必须对采用 4 层 PCB 设计的系统的性能进行评估。

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9.2 封装信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD3138ARGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARJAR	Active	Production	VQFN (RJA) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARJAR.A	Active	Production	VQFN (RJA) | 40	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARJAT	Active	Production	VQFN (RJA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARJAT.A	Active	Production	VQFN (RJA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARMHR	NRND	Production	WQFN (RMH) | 40	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARMHR.A	NRND	Production	WQFN (RMH) | 40	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARMHT	NRND	Production	WQFN (RMH) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A
UCD3138ARMHT.A	NRND	Production	WQFN (RMH) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

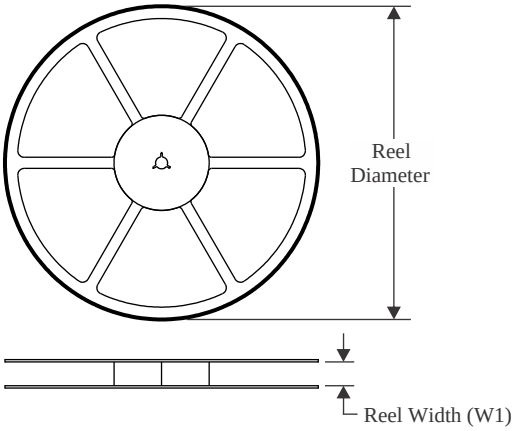
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

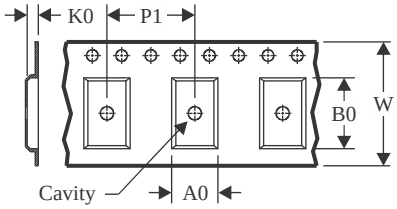
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

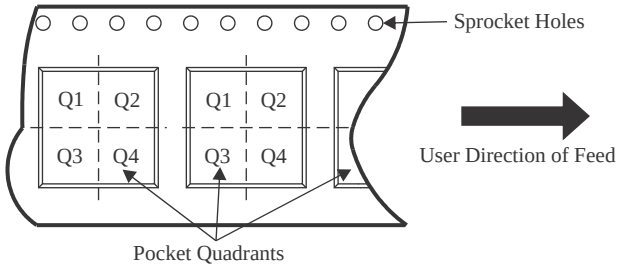


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

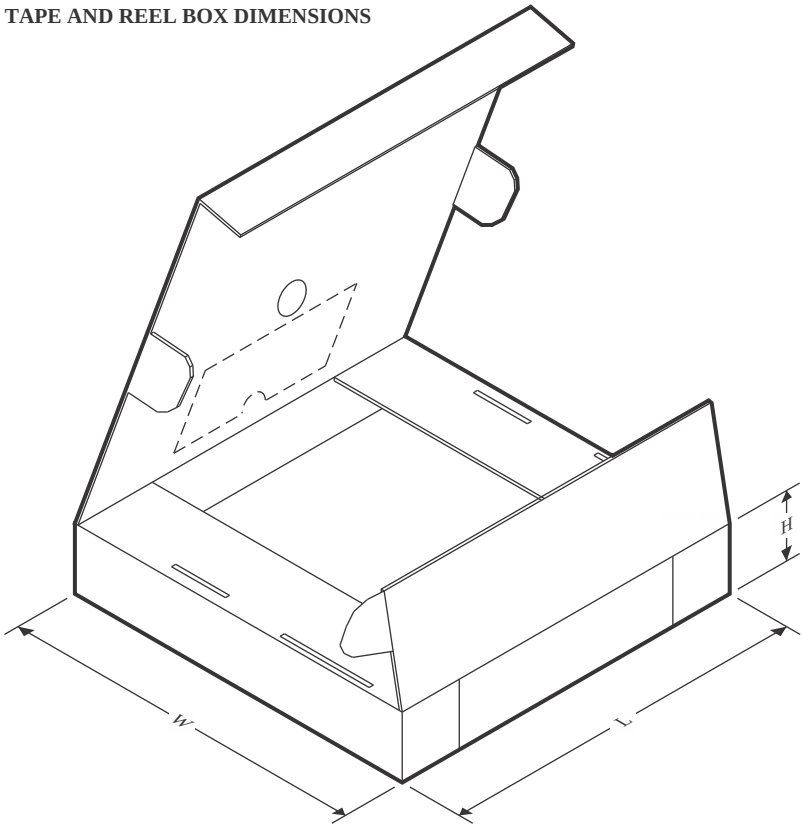
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD3138ARGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD3138ARGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD3138ARMHR	WQFN	RMH	40	2000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
UCD3138ARMHT	WQFN	RMH	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD3138ARGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD3138ARGCT	VQFN	RGC	64	250	210.0	185.0	35.0
UCD3138ARMHR	WQFN	RMH	40	2000	367.0	367.0	38.0
UCD3138ARMHT	WQFN	RMH	40	250	210.0	185.0	35.0

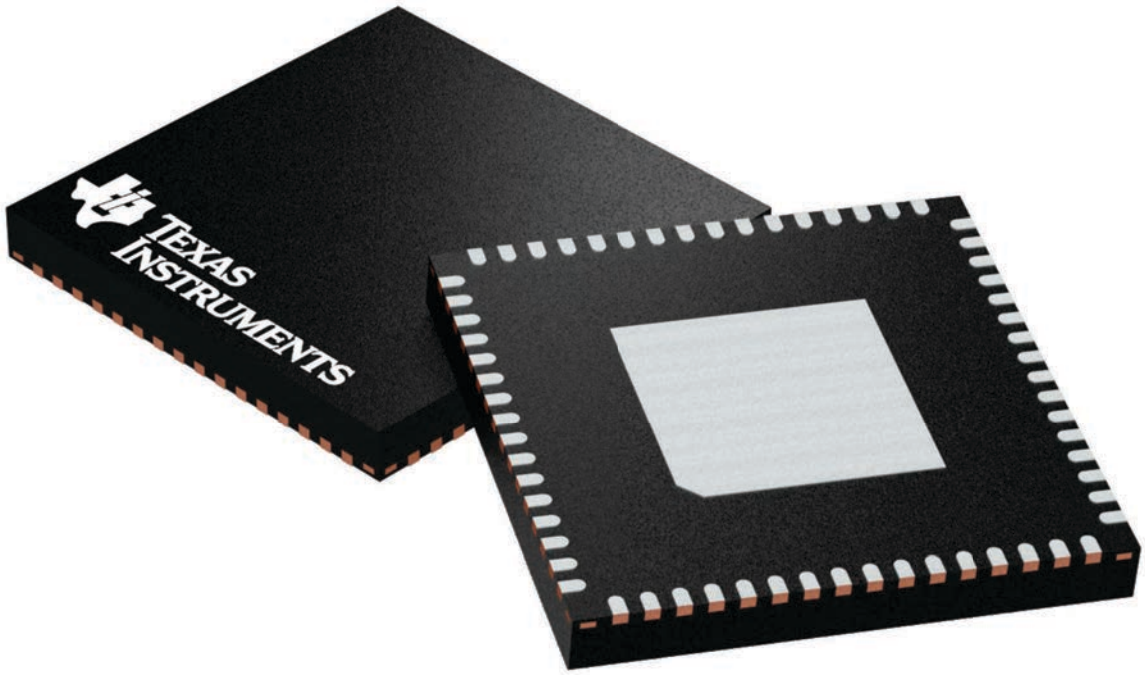
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

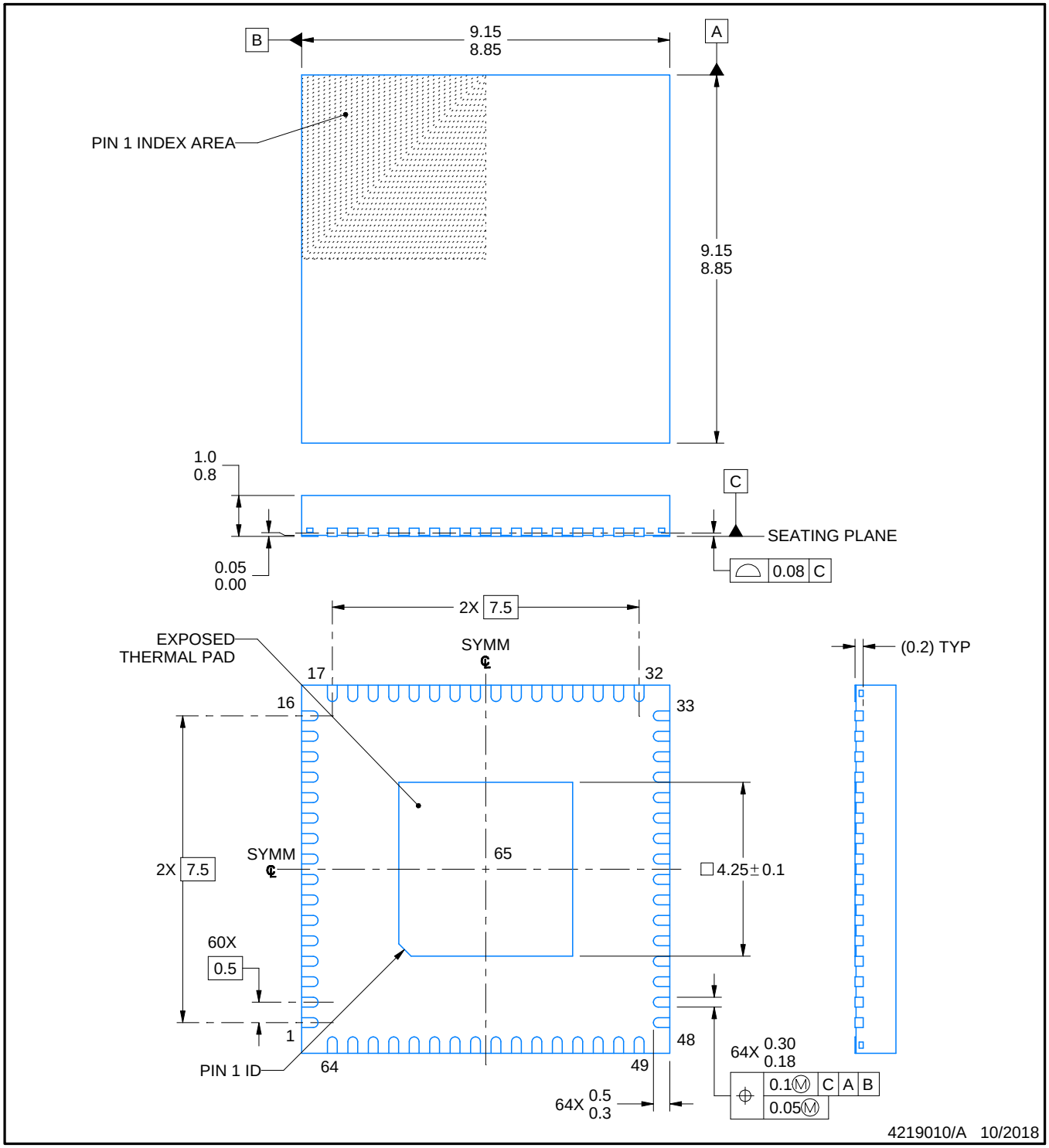
4224597/A

PACKAGE OUTLINE

RGC0064B

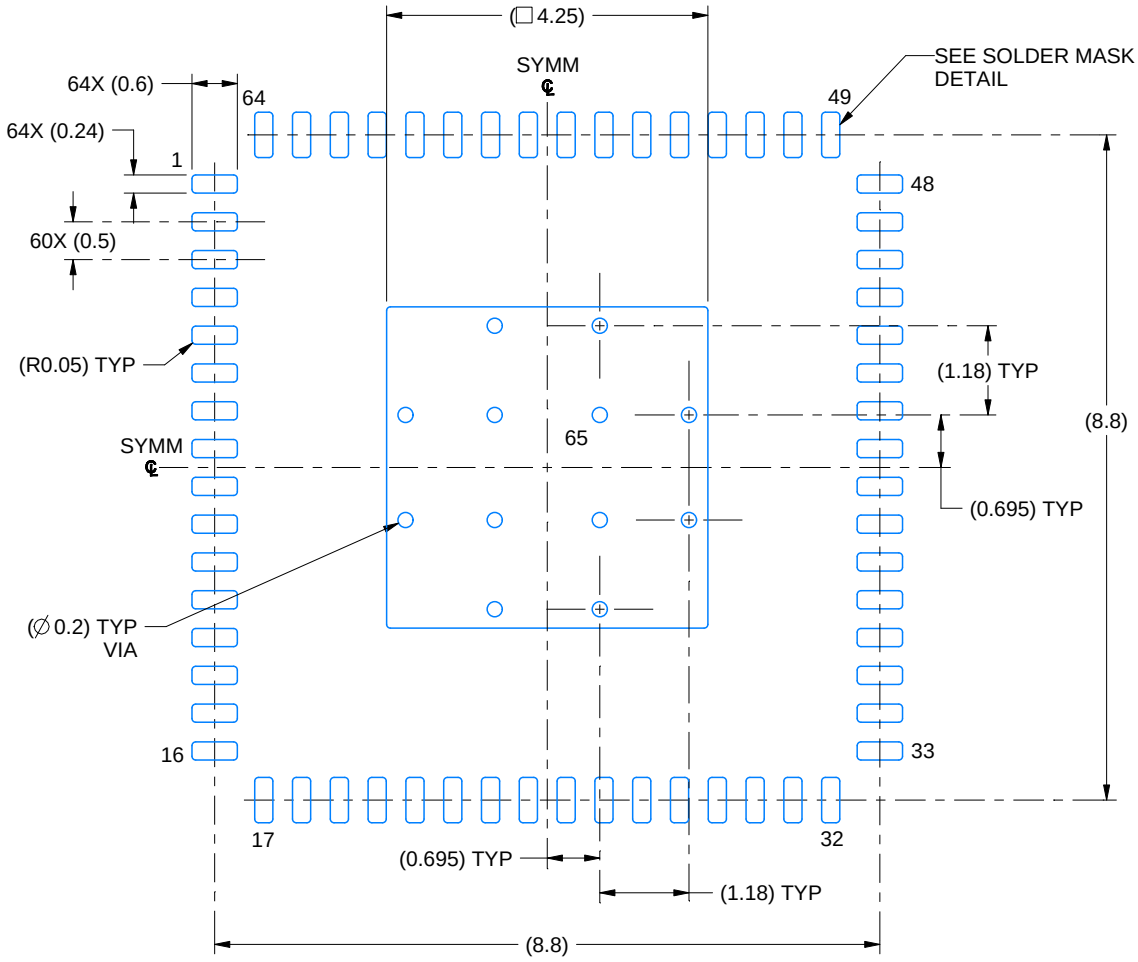
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

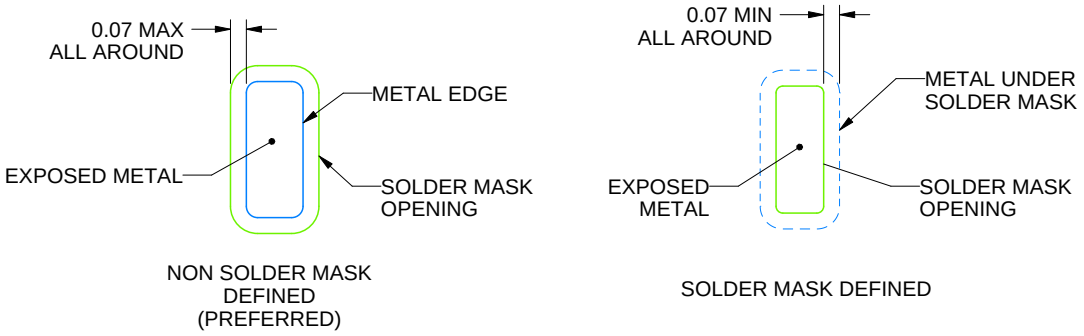


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

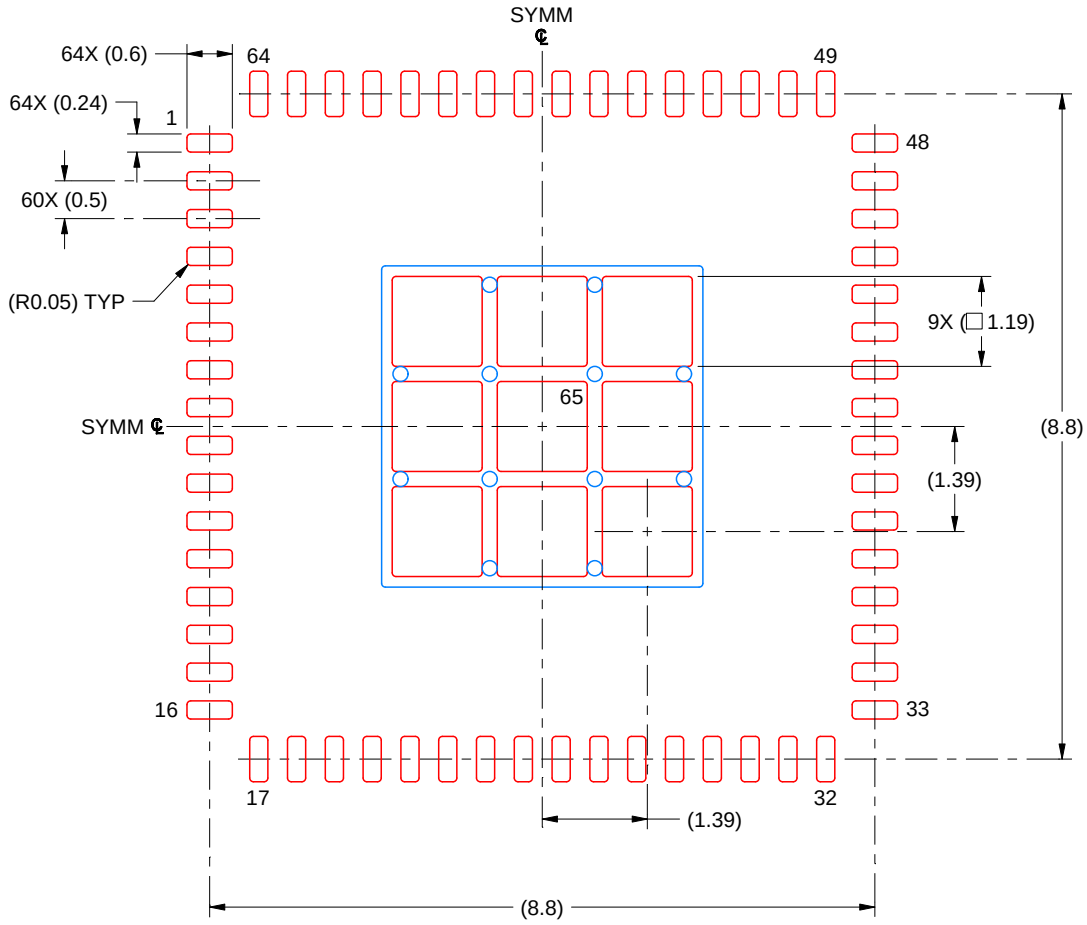


SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

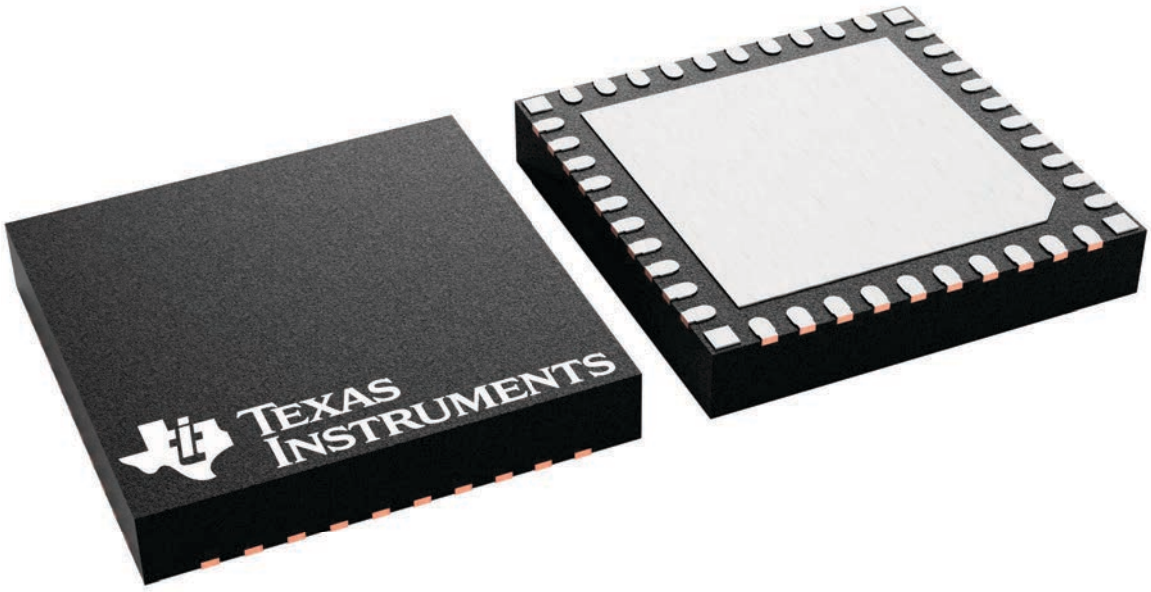
RJA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



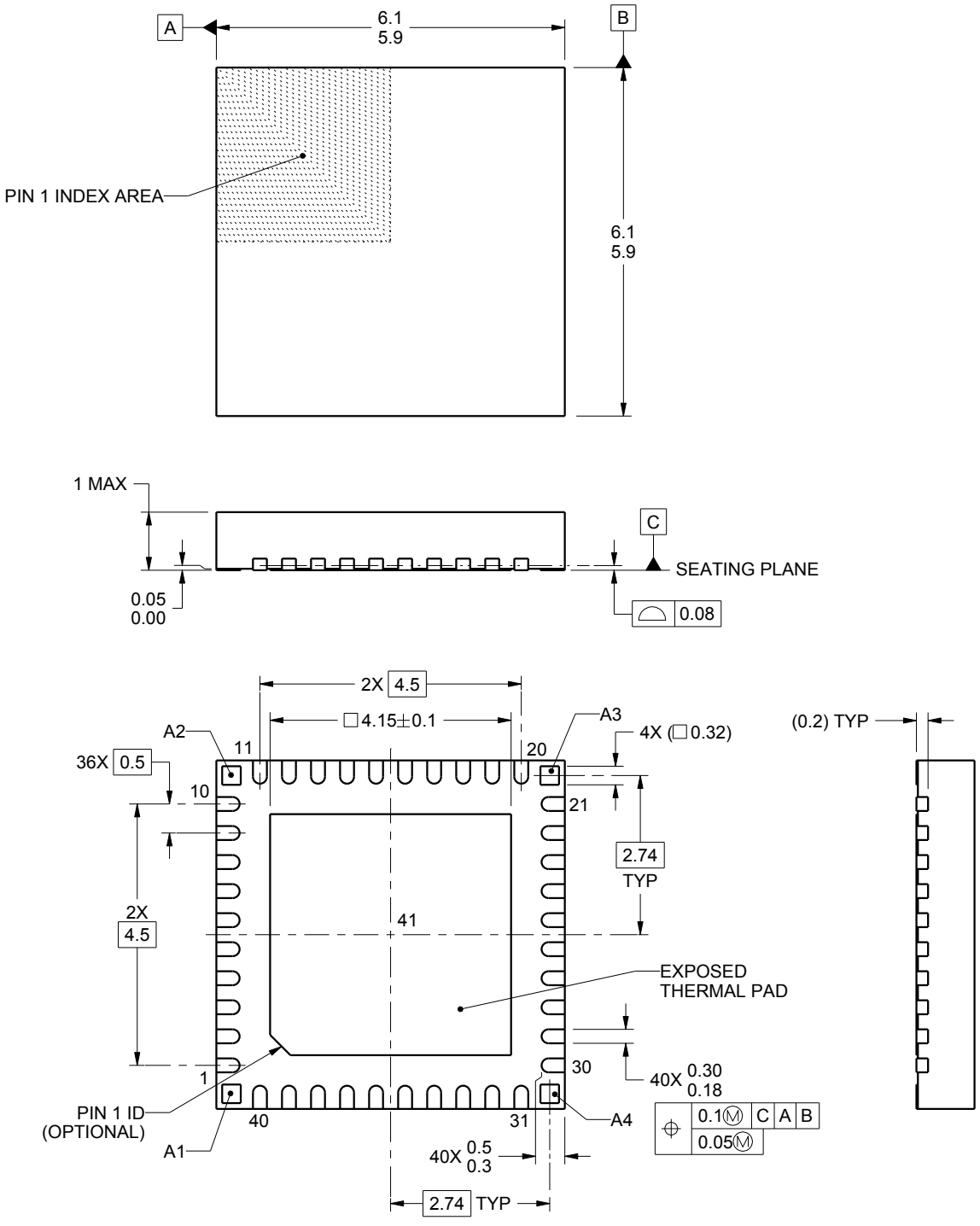
4231077/A

PACKAGE OUTLINE

RJA0040A

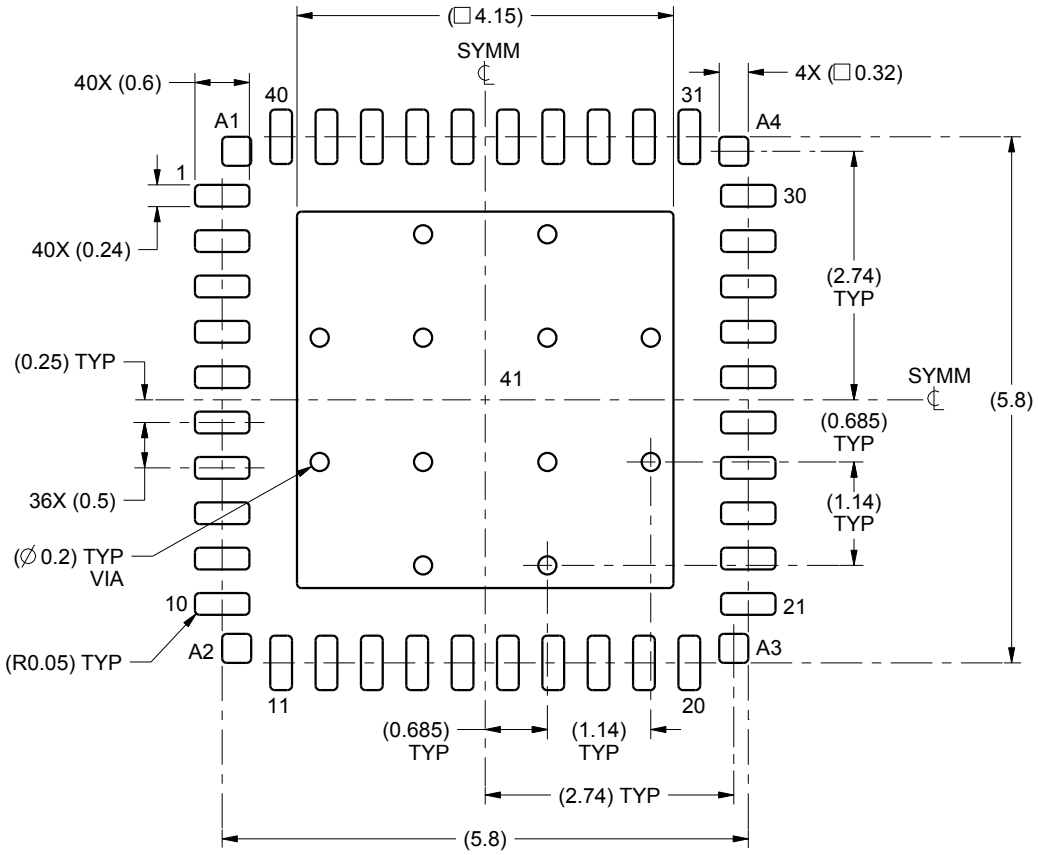
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

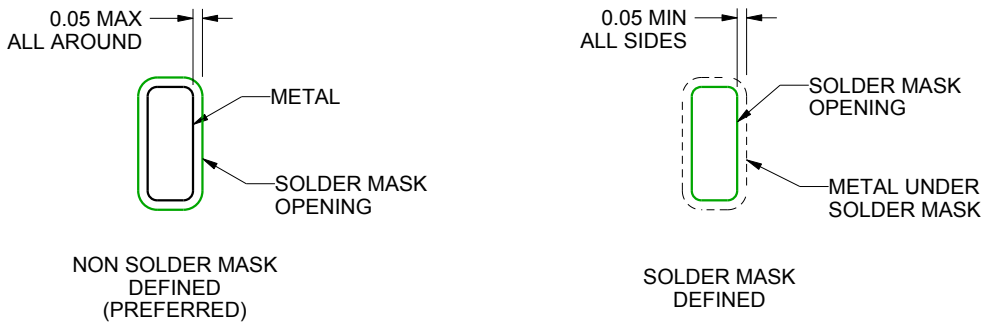


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X

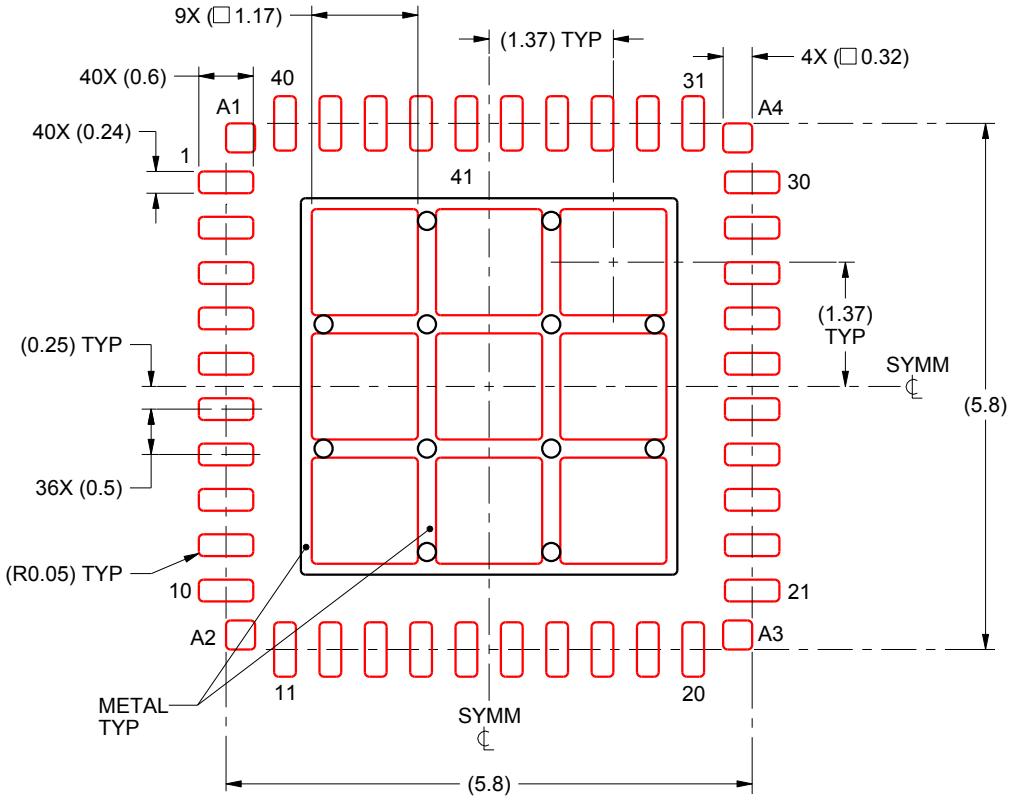


SOLDER MASK DETAILS

4222901/A 05/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

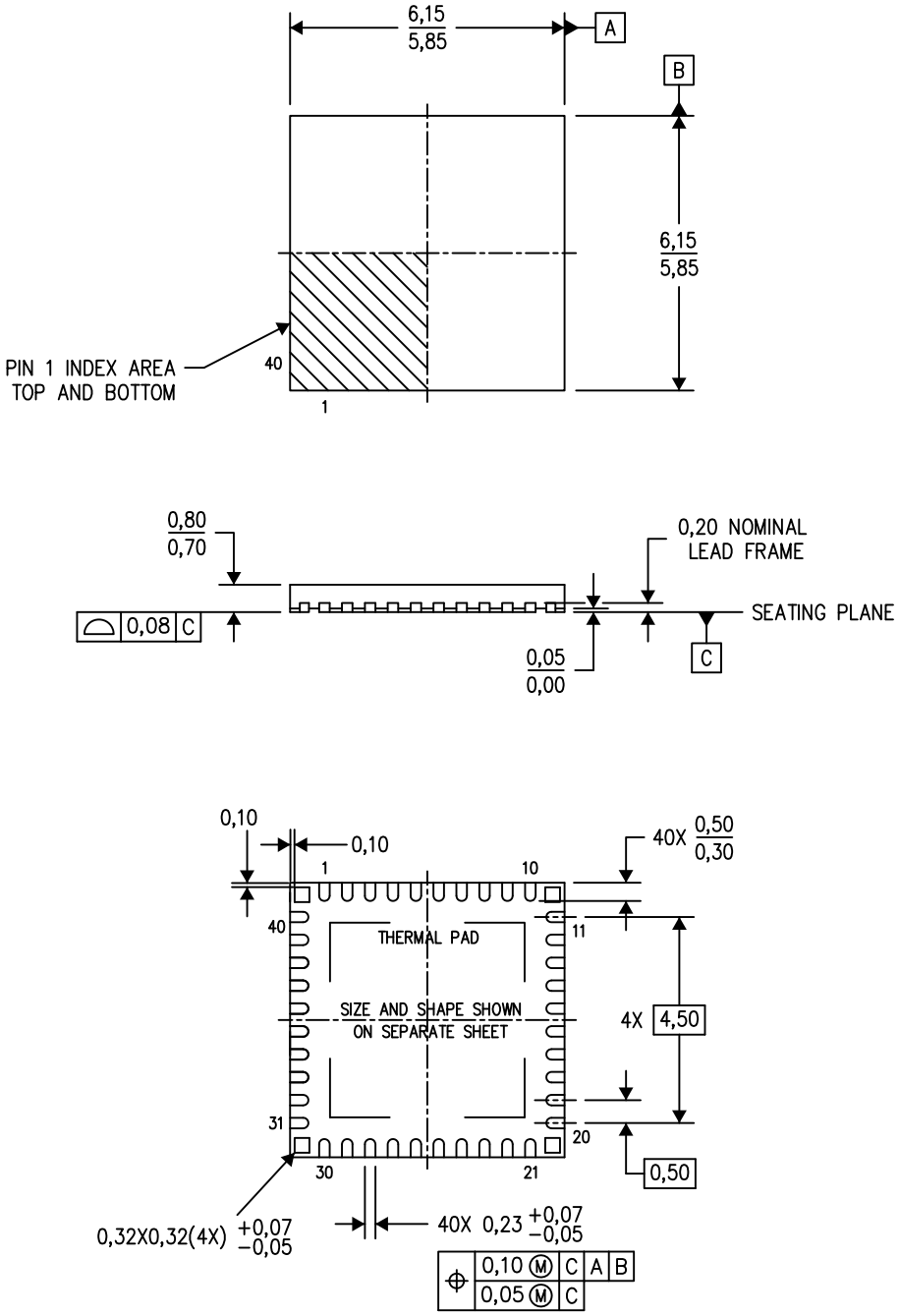
EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4222901/A 05/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RMH (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4218680/B 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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